INSTRUCTION MANUAL

BOXCAR INTEGRATOR

Model 160

MP MASTER
MA30246

INSTRUCTION MANUAL

BOXCAR INTEGRATOR

Model 160

THIS MANUAL APPLIES SPECIFICALLY TO MODEL 160 SERIAL NO.

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Princeton Applied Research Corporation
Princeton, New Jersey

NOTE: Material relating to changes, if any, will be found in envelope at rear of manual.

M124; 10/69

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SECTION I
CHARACTERISTICS

1.1 INTRODUCTION

The PAR™* Model 160 high-resolution Boxcar Integrator uses a sampling and averaging technique to extract synchronous waveforms from noise.

In essence, this instrument synchronously samples an input signal with a variable width, variable delay gate, which can be fixed at any point on, or slowly scanned across the input signal. That signal passed by the gate is averaged by variable time constant integrators, the output of which is the average of some number of repetitions of the input signal over the gate width interval. Because the average value of noise over a large number of repetitions is zero, an improvement in signal-to-noise ratio occurs. If the gate is fixed on a single point of the input signal, the Model 160 output rises asymptotically toward the amplitude of the synchronous portion of the input signal at the sampled point. If the gate is scanned across the input signal, the synchronous waveform is reproduced at the output.

Featuring a wide range of time constants, gate widths, and scan rates, along with good hold time and stability, the Model 160 should be of value in any application where noise interferes with the recovery of repetitive waveforms.

* PAR is a trademark of Princeton Applied Research Corporation.

1.2 SPECIFICATIONS

SIGNAL CHANNEL

(1) INPUT SENSITIVITY

±50 mV to ±10 V in 1-2-5 sequence for ±10 V output. Relative attenuator accuracy is better than ±0.5%.

(2) INPUT COUPLING

AC, DC, or GRD.

(3) INPUT IMPEDANCE

100 kilohms or 50 ohms, switch selectable, separate input jacks provided.

COUPLING	100 kΩ INPUT	50Ω INPUT
DC ------ AC ------ GRD. ----	100 kΩ paralleled by 50 pF 1 μF in series with 100 kΩ. 1 μF in series with 10 MΩ.	dc coupled 50 ohms (±2%) regardless of position of Coupling switch.*

(4) MAXIMUM INPUT VOLTAGE

50 ohm input --- 10 V rms, 20 V peak.
100 kΩ input --- 200 V peak.

(5) PREFILTER BANDWIDTH (-3 dB)

(a) Type Filter - Single-section, low-pass filter providing a -6 dB/octave rolloff.

(b) Bandwidth - dc to 3 kHz through 30 MHz in 1-3-10 sequence. Bandwidth accuracy is ±10%.

(c) OFF bandwidth - dc to 50 MHz (typical).

(6) INPUT OFFSET

±100% or ±1000% of full scale. Calibrated to ±2% accuracy.

(7) NOISE

Internally generated noise is a function of aperture time, duty factor, and time constant. Typically, the output noise is less than 0.03% rms of full scale.

*Although the input resistance is 50 ohms direct, the internally processed signal will be "AC", "DC" or "GROUND" coupled, according to Coupling switch position.

(8) DC DRIFT

Typically 0.03% of full scale per degree Celsius. Twenty-four hour drift at constant ambient temperature is less than 0.2% of full scale after a two-hour warm-up.

(9) GAIN STABILITY

±0.5% of full scale per week, maximum.

(10) LINEARITY

Less than ±0.25% of full-scale error for signals within the full scale range. For input signals exceeding full scale, the linearity is degraded to ±2% of maximum input up to 10 times full scale in the normal resolution mode and three times full scale in the high resolution mode.

(11) OUTPUTS (relative to full-scale input)

(a) Panel Meter - ±1% linear, center zero. The scales on the meter correspond to the selected sensitivity.

(b) ±10 V dc at 1000 ohms. Two of these outputs are provided, one normal and the other inverted.

(c) ±1 mA for low impedance recorders.

(d) Preamplifier output: ±0.5 V at 300 ohms*. With 50 ohm load, output is nominally ±70 mV.

SAMPLE-HOLD CHARACTERISTICS

(1) APERTURE TIME (Gate Width)

(a) High Resolution Mode - Continuously variable from 10 ns to 5.5 μs in three ranges. Accuracy is ±10% of range.

(b) Normal Resolution Mode - Continuously variable from 0.5 μs to 0.55 s. Accuracy is ±10% of range.

(2) AVERAGING TIME CONSTANTS

(a) High Resolution Mode - 3 ns to 1000 μs in 1-3-10 sequence. Time constant may be effectively increased to at least one second by using the Stretch Time switch and Normal Resolution time constant.

(b) Normal Resolution Mode - 0.1 ms to 100 s in 1-3-10 sequence. Also 0.01 ms. Provision for determining time constant with external capacitor.

*±1 V at 600 Ω in early units.

(3) HOLDING TIME (Memory Drift)

The holding time is a function of the setting of the Time Constant, Aperture Time Mode, and Retention controls. The drift is typically linear with time and it can be expressed as a percentage of full-scale output change per second.

(a) Normal Resolution Mode

$$\text{Memory Drift (typical)} = \frac{\text{5 ppm of full scale per second}}{\text{Time Constant}}$$

or, tabularized:

Time Constant	Memory Drift (typical) % of full scale per 100 seconds
.01 ms	5
.1 ms	5
.3 ms	2
1 ms	0.5
3 ms	0.2
10 ms	0.1
30 ms	0.05
100 ms	0.01
.3 s	0.01
1 s	0.01
3 s	0.01
10 s	0.01
30 s	0.01
100 s	0.01

(b) High Resolution Mode - Memory drift is reduced to the drift characteristics of the previously specified normal resolution Time Constant settings providing the Retention control is optimally adjusted. This relationship is shown in the following table.

Time Constant	Memory Drift (maximum) % of full scale per second	
	Retention off	Retention optimal
3 ns	300	0.05
10 ns	300	0.05
30 ns	300	0.05
100 ns	30	0.05
300 ns	30	0.05
1 µs	1	0.05
3 µs	1	0.05
10 µs	1	0.05
30 µs	0.1	0.05
100 µs	0.1	0.05
300 µs	0.05	0.05
1000 µs	0.05	0.05

TIMING AND CONTROL

(1) TRIGGER MODES

(a) External - The timing and delay sequence is initiated by an externally derived waveform greater than 0.3 V and less than 5 V and having a rise time of 10 ns or slower. The maximum trigger repetition rate is 250 kHz.

(b) Recurrent - Unit triggers automatically and repetitively at approximately the reciprocal time base.

(2) DELAY RANGE

The delay between triggering and aperture opening is continuously adjustable from 5% to 100% of the Time Base Period. The delay is set by means of a ten turn calibrated dial and has a relative accuracy of ±0.5% of the Time Base. Provision is made for remotely adjusting the delay by applying an externally derived 0-to-10 volt positive dc signal. The jitter is either 1 ns rms or 0.05% rms of the Time Base, whichever is greater.

(3) TIME BASE

(a) Internal - 2.0 μs to 20 s in 1-2-5 sequence. Accuracy is ±5%. Linearity is typically ±1% from 10% to 95% of the Time Base.

(b) External - Provision is made for applying an externally derived zero to plus ten volt ramp. The external Time Base may be as fast as 10 V/μs for a delay accuracy of 2% or better.

(4) DELAYED TRIGGER OUTPUT

A pedestal is provided with an amplitude of one volt minimum into fifty ohms and a risetime of 25 ns or faster. The leading edge of the pedestal can begin anywhere between 5% and 100% of the Time Base. The trailing edge is simultaneous with the end of the Time Base. The pedestal may be manually positioned at a fixed percentage of the Time Base range or may be automatically scanned in synchronization with the aperture delay. Automatic scanning of Delayed Trigger output not available in early units.

(5) AUTOMATIC SCAN

(a) Scan Mode - The aperture delay is automatically scanned over any incremental portion of the Time Base Period. Full-scale scan periods range from one minute to 1000 minutes in 1-2-5 sequence. Scan period accuracy is ±15%.

(b) Scan Hold - Automatic scan may be stopped at any point and held.

(c) External Scan/Delay - An externally derived zero to +10 V signal will provide aperture delay over the range of the Time Base. The input impedance is nominally 5000 ohms.

GENERAL

(1) POWER REQUIREMENTS

105 to 130 Vac or 210 to 260 Vac, 50-60 Hz, 50 volt-amperes maximum.

(2) OUTPUT POWER

The following voltages are available at the rear-panel interface connector, allowing external accessories or external equipment to be powered by the Model 160.

Pin	Voltage	Accuracy and Regulation	Maximum Available Current
B	+24.0 V	±10 mV	50 mA
C	-24.0 V	±20 mV	50 mA
E	+12.0 V	±20 mV	50 mA
F	-12.0 V	±20 mV	50 mA
D	+ 4.7 V	±250 mV	50 mA
A	0 V	Power Ground Reference	
J	- 200 V*	±20 V	0.5 mA

(3) SIZE

(a) 19 inches wide, 7 inches high, and 15 inches deep.

(b) Unit is supplied with nineteen inch relay rack mounting fixtures.

(c) Weight - 43 lbs.

(4) OPTIONS (consult the factory for more specific information)

(a) Analog Storage Accessory, Model 161.

(b) Preamplifier, Model 115.

(c) Pre-Sampler.

ANALOG STORAGE MODULE SPECIFICATIONS

The Model 161 Analog Storage Accessory improves the memory drift charac-

*-200 V not provided in early units.

teristics of the Model 160 Boxcar Integrator when making low duty factor examinations of signals having a low repetition rate.

(1) MEMORY DRIFT

±0.05% of full scale per 100 seconds. Memory drift is independent of time constant.

(2) TRIGGER INPUT RATE

100 Hz maximum. Instrument "ignores" faster input triggers when Analog Storage is active (Memory switch to ON). However, with faster trigger rates, there is no need to use the Analog Storage capability.

(3) DUTY FACTOR LIMIT

Duty factor limit is a function of the integration time constant as explained in subsection 3.4G, page III-19.

SECTION II
INITIAL CHECKS

2.1 INTRODUCTION

The following procedure is provided to facilitate initial performance checking of the Model 160 Boxcar Integrator. In general, this procedure should be carried out after inspecting the instrument for shipping damage (any noted to be immediately reported to the carrier and to Princeton Applied Research Corporation), but before using the instrument experimentally. This procedure presupposes no detailed knowledge of the instrument or its circuitry on the part of the checker. Should any difficulty be encountered in carrying out these checks, contact the factory or one of its authorized representatives (see list at end of this manual). Locating the controls, switches, etc. may be facilitated by referring to the illustrative foldout on page III-43.

2.2 EQUIPMENT NEEDED

Most of the checks are self checking in that no special equipment is required to determine that the instrument is properly performing its primary functions. The following equipment, however, is recommended to carry out the complete checkout procedure.

(1) Square-wave source capable of furnishing 0-to-5 V and 0-to-10 V square waves. Suitable sources include TEKTRONIX type 114 Pulse Generator or calibrator output of most TEKTRONIX oscilloscopes, such as the type 545.

(2) Watch with a second hand, or a stop watch.

(3) Coaxial cables (3). Cables should have a characteristic impedance of 50 ohms and should be fitted with a BNC connector at each end.

2.3 PRELIMINARY STEPS

(1) Check the position of the rear-panel Line Voltage Selector switch. For operation from 115 Vac, "115" should show in the window. For operation from 230 Vac, "230" should show.

(2) Plug in the line cord and turn the Power switch on. The meter should be indirectly illuminated. The meter reading may be either off or on scale, depending on the setting of the front-panel controls. Allow about five minutes for the instrument to warm up and stabilize before proceeding to the following checks.

2.4 CHECKS IN THE CONTINUOUS TRIGGER MODE

(1) Set the front-panel controls as follows.

Trigger Mode ---------- CONT. GATE
Time Constant (red scale) ---------- .1 mSEC.
Input Coupling ---------- GRD.
Input Sensitivity ---------- 10 VOLTS
Offset Scale switch ---------- X1 F.S.
Offset Polarity switch ---------- OFF

(2) Zero Control Check

Adjust the Zero Control (not the Offset Dial) over its full range. Observe that the panel meter indication tracks the control setting. When the control is fully counter-clockwise, the meter indication should exceed negative full scale. When the control is fully clockwise, the meter indication should exceed positive full scale. Set the control for exactly a center scale deflection (zero indication).

(3) Gain Check

Having carefully set the Zero control for center scale deflection (zero indication), turn the Sensitivity switch to CAL. The meter should indicate positive full scale plus or minus two percent. If the meter deflection is off by more than ±2% but less than ±10%, it is possible that the setting of the internal Gain adjustment was disturbed in shipment. Because this does not interfere with the remaining checks, proceed to complete the initial checks. Then contact the factory (or an authorized representative) for advice or assistance in calibrating the gain. If the meter indication is off by more than ten percent, plus or minus, the instrument is definitely malfunctioning. Should this be the case, turn off the power and contact the factory (or an authorized representative) before taking any further action.

(4) Offset Check

Reset the Sensitivity switch to 10 V and set the Input Offset dial to 10% (one full turn from the fully counter-clockwise position). Then set the Offset Polarity switch to POS. The meter should indicate approximately 10% of full-scale positive. Carefully note the indication. Then set the Offset Polarity switch to NEG. The meter indication should be negative and its magnitude should be within one percent of full scale of the positive indication noted when the Offset Polarity switch was set to POS. Now set the Offset Scale switch to X10 F.S. The meter indication should increase by about a factor of ten.

2.5 CHECKS IN THE EXTERNAL TRIGGER MODE

(1) Set the front-panel controls as follows.

Trigger Mode ---------- EXT.
Aperture Time
Range ---------- .1 µSEC. (red)
Dial ---------- 30
(Aperture time = .1 µSEC. x 30 = 3 µSEC.)

Prefilter ---------- OFF
Time Constant (red)* ---------- .1 mSEC.
Time Base ---------- 2 mSEC.
Time Base Mode ---------- INT.
Trigger Slope ---------- +
Trigger Threshold ---------- midway between "0" and fully clockwise.
Initial Delay Dial ---------- 5%
Final Delay Dial ---------- 100%
Delay Mode ---------- DELAY
Scan Rate ---------- 1 minute
Input Coupling ---------- AC
Sensitivity ---------- 5 VOLTS
Input Selector ---------- 100 kΩ
Offset Polarity ---------- OFF
Delayed Trigger Mode** ---------- DIAL
Memory ---------- OFF

(2) Manual Delay Check

(a) Connect a zero to plus five volt, 1 kHz square wave (oscilloscope calibrate output) to the Trigger IN jack and to the 100 kΩ Input jack. The panel meter indication should be in the range of +2 V (40% of full scale) to +3 V (60% of full scale), depending on the source impedance and accuracy of the input square wave. [A highly accurate square wave from a low impedance source would give a meter indication of +2.5 V (50% of full scale)].

(b) Begin turning the Initial Delay dial slowly clockwise. As the dial is turned there should be no change in the meter indication until the dial setting reaches 25% (±5%), at which point the meter indication should suddenly swing negative to about the same degree as the positive indication noted in the previous step.

(c) Continue turning the dial. The meter indication should remain unchanged until the dial setting reaches 50% (±5%) at which point the meter indication should suddenly return to its original positive indication.

(d) Reset the Initial Delay dial to its initial 5% setting.

(3) Delayed Trigger Output Check

(a) Disconnect the square-wave input signal from the 100 kΩ input but leave it connected to the trigger input.

(b) Connect a cable between the Trigger DELAYED OUT jack and the 50

* Set in previous step.

**This switch not provided in early units.

ohm input jack. Then set the Input Selector switch to 50 Ω, the coupling switch to dc, and the Input Sensitivity switch to 2 V. Finally, set the Output Trigger Delay dial to 50%.

(c) Slowly rotate the Initial Delay dial from 5% to 100%. Initially the meter indication should be 0 V ±0.2 V. As the dial is rotated, this indication will not change until the dial setting reaches 50% (±10%), at which point the meter indication will swing to +1.2 V (+60% of full scale).

(d) Reset the Initial Delay dial to 5%.

(4) Scanned Delay Check

(a) Set the Delay Mode switch to SCAN and the Scan Repeat/Single toggle switch to SINGLE.

(b) Hold in the Scan Reset button and note the meter indication. It should be about 0 V.

(c) Using a stop watch or a pocket watch with a sweep second hand as an elapsed time indicator, release the Scan Reset button at some convenient time and note how much time passes between the time the button is released and the time the meter indication swings from 0 V to about +1.2 V. The elapsed time should be 30 seconds (±10 seconds).

2.6 CHECKS IN THE HIGH RESOLUTION MODE

(1) Set the front-panel controls as follows.

Trigger Mode*	EXT.
Trigger Threshold	fully clockwise
Delay Mode	DELAY
Time Base Mode*	INT.
Trigger Slope*	+
Initial Delay*	5%
Final Delay*	100%
Scan Rate*	1 minute
Trigger Delay*	50%
Trigger Delay Mode*	DIAL
Aperture Time	
Range	10 nSEC. (blue)
Dial	30
(Aperture time = 10 nSEC. x 30 = 300 nSEC.)	
Time Constant	1 µSEC. (blue)
Time Constant	.01 mSEC. (red)
Stretch Time	10 µSEC.
Retention	OFF
Prefilter*	OFF

*Set in previous step.

Input Sensitivity* ---------- 2 V
Input Selector* ---------- 50 Ω
Input Coupling* ---------- DC
Offset Polarity* ---------- OFF
Memory* ---------- OFF

(2) Increase the amplitude of the square wave signal being applied to the Trigger IN jack from zero-to-five volts to zero-to-ten volts.

(3) While noting the meter indication, slowly rotate the Initial Delay dial clockwise. The meter indication should remain near zero until the dial setting is approximately 50%, where the meter indication should suddenly increase to about +1.2 V (60% of full scale).

2.7 CHECKS IN THE RECURRENT MODE

(1) After disconnecting all previously connected signal cables, set the front-panel controls as follows.

Trigger Mode ---------- RECURRENT
Time Base ---------- 1 SEC.
Time Base Mode* ---------- INT.
Initial Delay Dial ---------- 50%
Final Delay Dial* ---------- 100%
Delay Mode* ---------- DELAY
Aperture Time
    Range ---------- 1 mSEC. (red)
    Dial ---------- 30
        (Aperture time = 1 mSEC. x 30 = 30 mSEC.)
Time Constant ---------- 1 SEC. (red)
Input Sensitivity ---------- 10 V
Offset Polarity ---------- OFF

(2) Depress the Memory Reset pushbutton switch and continue to hold it down. Then, while holding down the pushbutton, set the Sensitivity switch to CAL. At some convenient time, release the pushbutton. Note that the meter deflects positively in "steps". After ten steps (approximately ten seconds), the meter indication should be 25% ±5% of full scale. Return the Sensitivity switch to 10 V. The meter indication will decrease toward zero, again in steps.

2.8 SIGNAL CHANNEL CHECKS

(1) Set the front-panel controls as follows.

Trigger Mode ---------- CONT. GATE
Initial Delay ---------- 0%
Final Delay* ---------- 100%
Delay Mode* ---------- DELAY
Time Constant ---------- 10 mSEC. (red)

*Set in previous step.

Input Coupling ---------- GRD.
Input Sensitivity ---------- 50 mV
Input Selector ---------- 100 kΩ
Offset Polarity ---------- OFF

(2) HIGH SENSITIVITY CHECKS

(a) Connect a cable from the Scan/Delay Output jack on the rear panel to the 100 kΩ Signal Input jack. Then adjust the front-panel Zero control for exactly zero indication.

(b) Set the Coupling switch to DC and carefully adjust the Initial Delay dial for exactly full-scale meter indication (50 mV). NOTE: This adjustment is very sensitive and only a slight rotation is required to achieve full scale output. Then successively set the Input Sensitivity switch to the 100 mV, 200 mV, and 500 mV positions, taking care to note the meter deflection each time the sensitivity is changed. The deflection for each position should be as indicated in the following table.

Sensitivity Setting	Meter Indication	Tolerance
50 mV	50 mV (full scale)	±0.5 mV
100 mV	50 mV (50% of full scale)	±1 mV
200 mV	50 mV (25% of full scale)	±2 mV
500 mV	50 mV (10% of full scale)	±5 mV

(3) LOW SENSITIVITY CHECKS

(a) Set the Sensitivity switch to 1 V and adjust the Initial Delay dial as required to obtain exactly full-scale meter indication. Then successively set the Input Sensitivity switch to the 2 V, 5 V, and 10 V positions, noting the lower meter deflection each time the sensitivity is changed. The proper reading and tolerance is indicated in the following table.

Sensitivity Setting	Meter Indication	Tolerance
1 V	1.00 V (full scale)	±0.01 V
2 V	1.00 V (50% of full scale)	±0.02 V
5 V	1.00 V (20% of full scale)	±0.05 V
10 V	1.00 V (10% of full scale)	±0.10 V

This completes the initial checks. If the Model 160 performed as indicated, one can be reasonably sure that it is not malfunctioning and that it meets or exceeds its specifications. In general, it is not necessary or desirable to perform any alignment procedure upon receipt of a new instrument.

SECTION III
OPERATING INSTRUCTIONS

3.1 INTRODUCTION

The Model 160 Boxcar Integrator is a sophisticated laboratory instrument whose operation is complex; many inter-related and often subtle factors must be considered to be assured of achieving optimum performance in each experimental situation. However, by carefully studying this section of the manual, the operator should acquire background sufficient to routinely handle even the most difficult signal recovery problems, providing they are within the capabilities of the instrument.

This section begins with a discussion of several preliminary considerations, such as installation, cooling, warm-up, and power requirements. The preliminary material is followed by a brief discussion, on the block diagram level, of how the instrument functions internally. Although it is not necessary to understand the internal operation of the Model 160, the insight gained thereby should aid in understanding the detailed operating instructions which follow. For those who are interested, a far more detailed description of the inner workings of the instrument is provided in Section IV. The detailed operating instructions constitute most of Section III, in which the key factors relevant to operating the instrument are considered, including control settings, restrictions, sources of error, optimization of experimental parameters, and many others. Subsection 3.6 (PITFALLS) discusses some of the "unexpected" problems an operator might encounter in using the Model 160. It might be wise to glance over "PITFALLS" before proceeding. At the end of the section is a series of tables which list the various controls, connectors, and indicator lamps, along with a brief statement as to the function of each. These tables, together with the foldout photograph of the front and rear panels on page III-43, serve as a handy "refresher reference". They can also be of considerable value to the "first time operator" who wants to become reasonably familiar with the instrument before using it experimentally.

3.2 PRELIMINARY CONSIDERATIONS

INSTALLATION

The Model 160 can be either bench or rack mounted, and, if rack mounted, may be equipped with slides to facilitate moving the instrument in and out of the rack. Suitable slides may be purchased from: JONATHAN MANUFACTURING COMPANY, 1258 TEANECK ROAD, TEANECK, NEW JERSEY.

To slide mount the Model 160, the following parts or their equivalents are required.

QUANTITY	ITEM
1 pair	STEEL BALL BEARING SLIDE, QUICK DISCONNECT, PART NO. 110 QD-16-1 or 110 QD-18-1 (the "16" and "18" refer to the length of the slide in inches).
4	MOUNTING BRACKET, PART NO. SP-0440

The instrument is supplied with the slide mounting holes already drilled in the sides. To gain access to these holes and mount the slides, remove the side covers, which slide off once the top and bottom covers have been removed. The top cover slides free after removal of the two screws located under the top cover "lip" at the rear of the instrument. The bottom cover slides free after removal of the two rear bumper feet, each of which is held in place by a single screw. To mount the slides, use 7/32", 10-32, nickel-plated steel, round-head or pan-head screws.

POWER REQUIREMENT

Approximately 50 volt-amperes at either 100-130 Vac or 200-260 Vac, 50-60 Hz, are required. Changeover from one operating voltage to the other is accomplished by operating a rear-panel slide switch.

GROUNDING

The chassis of the Model 160 is internally connected to the "third wire" or grounding pin of the input power connector. IT IS ABSOLUTELY IMPERATIVE THAT THE GROUND PIN BE CONNECTED TO A GOOD EARTH GROUND CONNECTION, EITHER THROUGH THE POWER DISTRIBUTION SYSTEM OF THE LABORATORY, OR AT LEAST TO A "COLD WATER PIPE", WHICH IN TURN HAS A GOOD GROUND CONNECTION. This precaution serves not only to minimize shock hazards, but also to prevent the entire chassis from being "driven" at some high ac voltage.

Should it be necessary to electrically isolate the input power to the instrument, use a good quality, electrostatically-shielded, isolation transformer. The chassis of the instrument should still maintain its earth-ground integrity by running a heavy wire (#18 AWG or larger) from the chassis to input neutral or to an earth-ground connection.

COOLING

No special cooling techniques are required. The internal temperature rise with free air circulating around the chassis and through the top and bottom cover vents is about 15°C. If the instrument is operated in an enclosed rack with other equipment, the ambient temperature within the rack snould not exceed 40°C.

WARM-UP

Although the instrument is operational immediately after being turned on, at least half an hour should be allowed for stabilization.

3.3 INTERNAL FUNCTIONING

Referring to Figure III-1, a block diagram on page III-3, note that the signal to be processed is applied to either of the two input jacks, 50 Ω or 100 kΩ. Following passage through a low-pass filter to band-limit the noise, the signal is attenuated by the Sensitivity switch attenuator and then applied to the following amplifier. How the signal is processed after amplification depends on whether the instrument is operating in the "normal" resolution mode (0.5 μs $\leq$ aperture time $\leq$ 0.55 s) or in the "high" resolution mode (10 ns $\leq$ aperture time $\leq$ 5.5 μs).

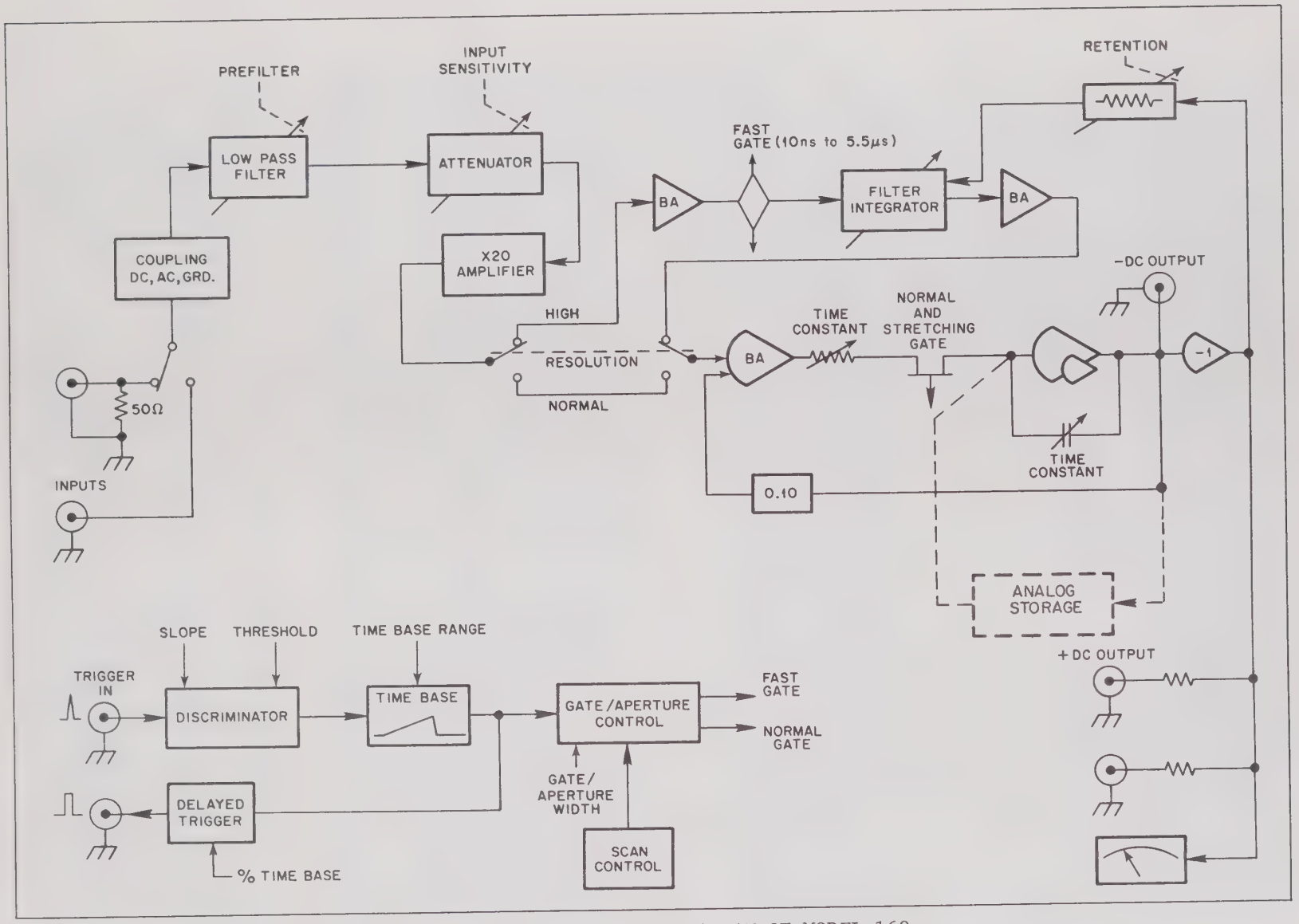


Figure III-1. SIMPLIFIED BLOCK DIAGRAM OF MODEL 160

In the normal resolution mode, the signal is routed to a buffer amplifier, the output of which is applied through a variable resistor to a solid-state switch (gate). This switch gates current to the summing junction of a chopper-stabilized amplifier connected as an analog integrator. Whenever the switch conducts, the entire circuit behaves as an integrator whose time constant is determined by the capacitance around the amplifier and the resistance between the gate and the output of the buffer amplifier.

A portion of the integrator output is fed back to the input of the buffer amplifier. As a result, the loop responds such that the integrator output asymptotically approaches the average of the applied signal. When the gating switch is closed (not conducting), the output "holds" at the last level reached when the switch was conducting. By opening the switch at the same time relative to each repetition of the input signal, and keeping it open for the same duration each time, the integrator output will asymptotically approach the average value of the input signal over the conducting interval. As this interval is normally very short, the output level gives one point-value on the input signal. If the gate-conducting interval is gradually scanned over the input signal, with the scanning rate sufficiently slow to allow the integrator to fully respond to every point on the input waveform, the entire input signal can be reproduced at the output with good resolution.

The integrator output, which is inverted with respect to the input signal, is routed directly to the rear-panel INVERTED OUTPUT jack. It is also routed to a final inverting amplifier, which provides the Output signal at a front panel connector, as well as the non-inverted or NORMAL Output signal at a rear panel connector.

In the high resolution mode the situation is somewhat different. The signal at the output of the gain-of-twenty amplifier, instead of being applied to the buffer amplifier which feeds the "normal" gate, is instead applied to a different buffer amplifier, the one which feeds the "fast" gate. Although the leakage characteristics of this gate are not as good as those of the normal gate, it has a much faster response time. The output of the fast gate is integrated and held in a high-impedance buffer amplifier. To compensate for the poorer hold characteristics of the fast gate, the buffer amplifier output is then applied to the normal gate, which in turn samples the fast gate output (stretches it) before it can decay. Additionally, a portion of the final output signal is fed back to the fast-sampler integrator such as to cause the fast-sampled and averaged signal to be retained for the maximum time possible. This positive feedback is optimized by means of the front-panel RETENTION control.

A number of timing circuits are required to "open" the gate(s) (cause them to conduct) at the proper time and for the proper duration. During operation in the External Trigger mode (the most commonly used mode), an input trigger pulse applied to the front-panel Trigger In jack is detected with respect to both amplitude and slope. The detected trigger causes a time base ramp to begin. The instantaneous value (voltage) of the time base ramp is compared with another dc voltage controlled by the setting of the Initial Delay dial, assuming the Delay Mode switch is in the DELAY position. When the two voltages are in time coincidence, a pulse is generated and sent to the Aperture Time circuits, which provide the "strobe" pulses to open one or both of the sampling gates according to whether the instrument is operating in the normal

or high resolution mode. If the Delay Mode switch is in the SCAN position, the voltage with which the time base ramp is compared is slowly increased at the selected SCAN RATE. As a result, the gate opening following each successive trigger pulse occurs slightly later, relative to the input trigger pulse, than did the previous gate opening. The processed waveform is then produced at the output as a function of the delay time. If the output voltage and the internally derived scan voltage are applied to the ordinate and abscissa drives respectively of an X-Y recorder, the resulting plot will be a time-scaled replica of the real time waveform.

3.4 DETAILED OPERATING INSTRUCTIONS

3.4A SYNCHRONIZATION

INTRODUCTION

A prime requirement in using the Model 160 is that the waveform to be processed be repetitive (though not necessarily periodic) and that a synchronizing signal precede the portion of the waveform to be examined. In addition, the synchronizing signal must bear a fixed constant time relationship to the waveform under investigation. As the most common method of implementing this requirement is to trigger the Model 160 with the stimulus which initiates the signal to be processed, this means of triggering will be considered first.

EXTERNAL TRIGGER MODE

When the Trigger Mode switch is set to EXT, an externally derived trigger signal must be applied to the front-panel Trigger In jack to initiate each time base ramp, delay, gate opening sequence. The Slope and Threshold controls determine when, in terms of the fine structure of the trigger pulse, the time base will be initiated. The Threshold control allows triggering over a range of ±5 V and the Slope control allows triggering on either the positive-going or negative-going edge of the input trigger. For reliable operation the applied triggers should be at least 300 mV in amplitude and of sufficient width to maintain the minimum amplitude-width product requirement of 10^{-8} volt-seconds. Do not apply trigger pulses larger than 50 V (zero-to-peak) because such pulses may damage the trigger discriminator circuitry.

Figure III-2 shows the variation in trigger detection point for two arbitrarily determined thresholds and for both slopes. The main criterion in setting these controls is to select a point which gives a stable trigger point for each input trigger pulse.

One might proceed as follows to establish proper synchronization in the external trigger mode.

(1) Apply the trigger waveform to the Trigger In jack and set the Trigger Mode switch to EXT.

(2) Select the desired slope and set the Initial Delay dial to 5%.

(3) Set the Time Base duration and Aperture Time controls as appropriate. Then set the Delay Mode switch to DELAY.

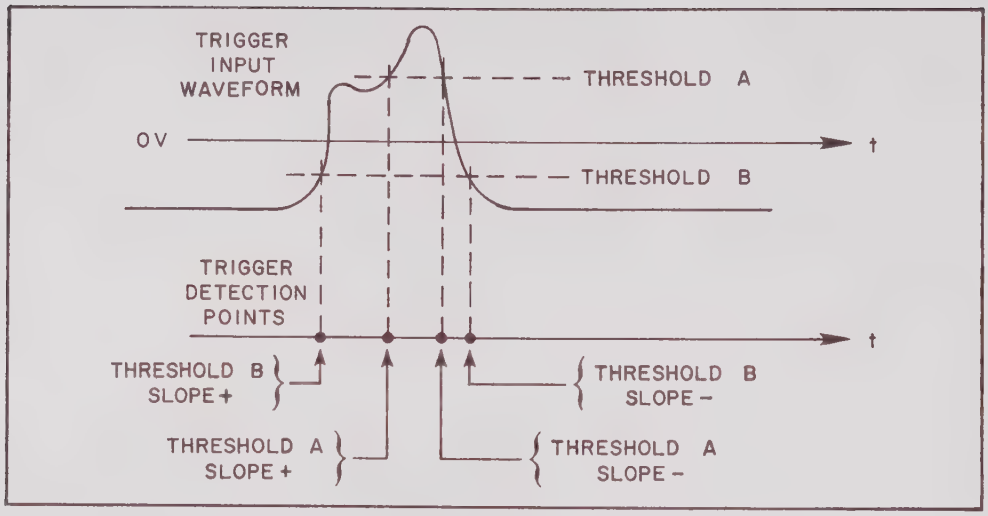


Figure III-2. TRIGGERING AS A FUNCTION OF SLOPE AND THRESHOLD

(4) Adjust the Threshold control as required to obtain stable triggering. Ways of determining that the Model 160 is triggering include the following.

(a) Note the responsiveness of the output. If the instrument is triggering properly, the output circuits and meter will be responsive to changes in the level of the input signal. The Sensitivity switch allows an appropriate "signal" to be applied. For example, changing the switch position from 10 VOLTS to CAL. introduces a full-scale input signal and should result in a corresponding deflection at the output. Similarly, the Zero and Offset controls also can be used to introduce a "signal". If the meter responds to changes in the setting of these controls, the instrument is triggering. If they do not, it is not triggering.

(b) Any of several timing outputs can be monitored with an oscilloscope. Usable outputs include the Delayed Trigger and Gate outputs on the front panel and the Time Base output on the rear panel.

(c) Another method is to make use of the Tilt light. If the Aperture Time is intentionally set wider than the Time Base, the Tilt light will flash when the instrument is triggering. Once proper triggering is established, the controls can be returned to their proper settings.

RECURRENT TRIGGER MODE

In the Recurrent Trigger mode (Trigger Mode switch set to RECURRENT) the time base circuitry "free runs" at a frequency approximately equal to the recipro-

cal of the time base period. Use of this mode allows the Model 160 itself to serve as the coherent trigger source. Either the rear-panel time base ramp output or the front-panel delayed trigger output can be used to trigger the "event" being studied. The ramp output is a positive-going ramp, whose quiescent voltage level is about -0.3 V. It rises linearly to about +10 V and then abruptly "flies back" to -0.3 V. In the simplest case, another ramp begins immediately. With certain control settings, however, the time base ramp behavior differs radically. The maximum voltage the ramp can attain is determined by the setting of the front-panel Final Delay dial. Only when the dial setting is 100% does the ramp reach +10 V. With lower dial settings the final voltage is proportionally less, as is the ramp duration. For example, if the dial setting is 50%, the ramp will "fly back" (reset) when it reaches +5 V and the ramp duration will be half that indicated by the symbolization of the Time Base Duration switch. Consequently, in the Recurrent Trigger mode, the repetition rate will be higher if the Final Delay dial setting is less than 100%.

If the instrument is being used in the high resolution mode, other factors serve to reduce the repetition rate. When one time base ramp ends, another cannot begin unless the stretch time interval has elapsed and the analog storage is completed. This latter condition applies only to units equipped with the analog storage accessory. Both the stretch time interval and the storage period begin coincident with the gate opening. Because the gate opening may be located, with respect to time, anywhere on the time base ramp, these periods of time base "inhibition" may or may not reduce the repetition rate in a given experiment.

CONTINUOUS GATE MODE

In the Continuous Gate mode the instrument no longer functions as a boxcar integrator. Instead, it becomes a straightforward amplifier whose frequency response is determined by the setting of the Prefilter and Time Constant (red) switches, and whose sensitivity is given by the setting of the Sensitivity switch. Only the normal resolution mode Signal Channel components are active and the FET Gate is "locked" into conduction.

DELAYED TRIGGER OUTPUT

The delayed trigger output is a zero-to-three volt (1.2 V into 50 ohms) positive pedestal. Its leading edge, relative to the beginning of the time base ramp, occurs anywhere along the time base ramp. Two modes of operation are provided, depending on the position of the Delayed Trigger Mode switch. If the switch is set to DIAL, the location of the leading edge is determined solely by the setting of the Output Trigger Delay dial, which is calibrated from 0% to 100% of time base. If the switch is set to SCAN, the leading edge of the pedestal automatically tracks the delay as established by the Initial Delay, Scan Rate controls, and Scan Mode switch (DELAY, HOLD, or SCAN). This scan, then, is identical to that which positions the aperture opening and is controlled from the front panel in the same manner (see 3.4B TIMING). The delayed trigger pedestal ends during the time base ramp reset as shown in Figure III-3. Two uses for this delayed trigger are: (1) to trigger the experiment when operating in the Recurrent Trigger mode, and, (2) to facilitate

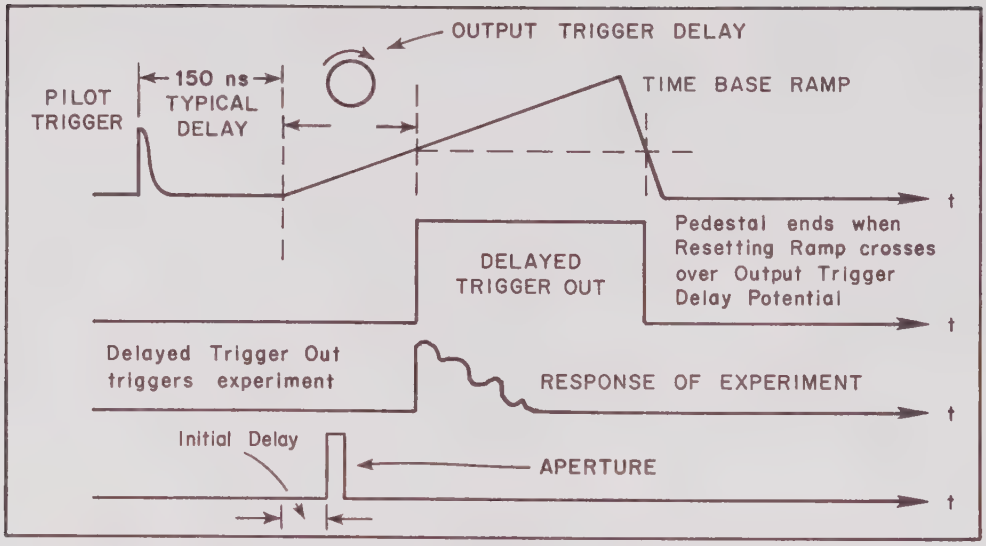


Figure III-3. USE OF DELAYED TRIGGER OUTPUT

the examination of phenomena which occur very soon after the prime trigger when operating in the External Trigger mode. This latter application is illustrated in Figure III-3. Note that a "pilot" trigger is used to trigger the Model 160 and initiate a time base ramp. At the point determined by the setting of the Output Trigger Delay dial, the delayed trigger pedestal begins. Its leading edge is used to trigger the experiment and a response waveform containing information very soon after the stimulus is generated as shown in the figure. The nearness of the information of interest to the stimulus poses no problem in this case because the aperture (gate opening period) can be located anywhere along the time base ramp, and, as indicated in Figure III-3, the 150 ns typical delay between triggering of the Model 160 and initiation of a time base ramp in no way interferes with recovery of the leading-edge information.

3.4B TIMING

Each time the Model 160 is triggered, either externally or recurrently, a time base ramp is generated. Some time after the beginning of the time base ramp, but before it ends, the sampling gates are strobed for a period equal to the selected aperture time, and the output of the Model 160 "corrects" toward the average value of the input signal over the aperture time interval. If the Delay Mode switch is set to DELAY, the delay between the start of the time base ramp and the gate strobe is determined by the setting of the Initial Delay dial, with the dial being calibrated as a percentage of time base to facilitate recording the time displacement between recovered "points" of the input waveform.

If the Delay Mode switch is set to SCAN, the delay between the beginning of the time base ramp and the strobe pulse is gradually increased with each successive trigger, with the rate of increase being determined by the selected scan rate. The delay is scanned over an interval determined by the setting of the Initial Delay dial and Final Delay dial. In other words, a scan be-

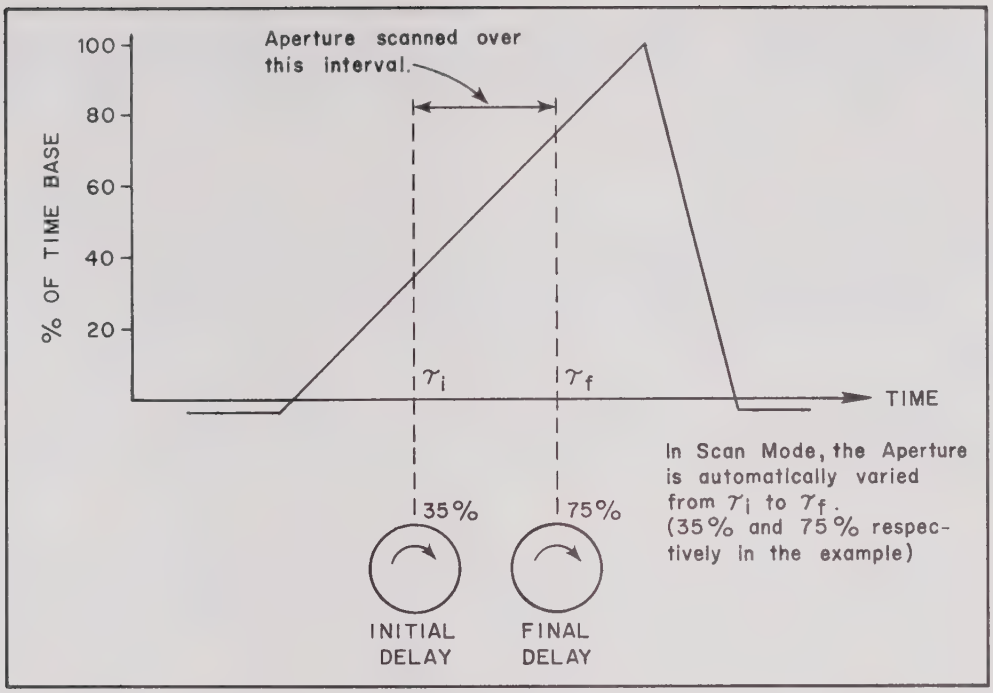


Figure III-4. TIME RELATIONSHIPS IN SCANNED DELAY MODE

gins with the aperture delay indicated by the setting of the Initial Delay dial. This delay then linearly increases, and finally "stops" at the delay indicated by the setting of the Final Delay dial. When the final delay is reached, the scan will either remain at that time (hold), or automatically reset to the initial delay to begin another scan. If the Repeat/Single switch is in the REPEAT position, the scan will automatically be repeated. If it is in the SINGLE position, the scan ends and holds at the final delay. A scan may be interrupted at any time by pressing the Scan Reset button or by quickly setting the Scan Mode switch to HOLD. In the first case (scan reset), the scan automatically resets to the initial delay. In the latter case (hold), the last value of delay holds and all successive gate openings occur at that delay. Figure III-4 illustrates these relationships.

The time required to scan from τ_i and τ_f is given by:

$$\text{Scan Time} = \text{Selected Scan Period} \times (\tau_f - \tau_i)/100,$$

where τ_i is the setting of the Initial Delay dial and τ_f is the setting of the Final Delay dial. For example, if the Scan Rate switch were set to 10 MIN, and the Initial and Final Delay dials were set to 65% and 75% respectively, the time required to scan over the 65% to 75% of time base interval would be:

$$\text{Scan Time} = 10 \text{ minutes} \times (75 - 65)/100 = \text{one minute}.$$

Note the parenthetical expression $(\tau_f - \tau_i)$ in the equation. If τ_f is made

less than or equal to τ_i, the scan does not reverse. This condition represents an operator error and will cause the TILT light to turn on. It should be noted, however, that during single scan operation the Tilt light comes on at the end of the scan, not to indicate an "error", but merely to remind the operator that the "run" is complete.

3.4C TIME BASE SELECTION

The choice of time base bears directly on the ability of the instrument to recover a given waveform. Ideally, the selected time base should be as short as possible (assuming external triggering) to minimize the effects of delay jitter. At the same time, the time base should not be so short as to cause important signal information to be "lost" because it falls, in time, outside the time base interval. Judicious use of the Final Delay dial allows the time base to be set to any value between those indicated by the Time Base Duration switch and thus allows efficient time utilization as illustrated in the following example.

Assume a repetitive waveform having a repetition period of 2.4 ms, with the point of interest located 2.1 ms after triggering. A time base period of 2.0 ms would be too short. A time base period of 5 ms would cause every other repetition of the input signal to be "skipped" (the instrument cannot be triggered with a time base ramp already in progress), with a resulting doubling in the time required to recover the information of interest. However, if one selects a time base of 5 ms and simultaneously sets the Final Delay dial to 44%, the time base duration will be reduced to 2.2 ms (44% of 5 ms = 2.2 ms), an ideal time base for the assumed input signal. When each time base ramp reaches 2.2 ms, it will automatically reset and the next trigger pulse will initiate another time base, thereby achieving the most efficient time use.

3.4D REPETITION RATE

Frequently it is neither necessary nor desirable that each trigger pulse initiate a time base ramp, as is the case if the experiment is being triggered by an oscillator whose period is shorter than the duration of the waveform being investigated. Where that is the situation, it is awkward (at the very least) to start a new time base ramp while another one is still in progress. Hence trigger pulses are prevented from starting time base ramps under the following conditions.

(1) A time base ramp is in progress.

(2) The gated signal is being "stretched" (10, 30, or 100 μs beginning with gate opening - applies to high resolution mode only).

(3) The aperture time "overlaps" the end of the time base period.

(4) The signal is being stored by the optional analog storage accessory (applies only to units equipped with this accessory). The storage period lasts about 5 ms and begins coincident with the gate opening.

Whether these last three conditions will inhibit in a given situation depends

on the position and duration of the aperture time relative to the time base duration. If the sum of the aperture time, stretch time, and storage period is sufficient to extend beyond the end of the time base, inhibiting will take place for the period of the "extension".

To illustrate these points, consider the following example. Suppose the desired time base were 20 µs and that scanning was desired from 5% to 100% of the time base. Further suppose the repetition period to be exactly 21 µs, and that one is operating in the high resolution mode with a 10 µs stretch period and an aperture time which is very short relative to the time base. Finally, consider the analog storage circuitry to be disabled (Memory switch to OFF). The effects of the time base inhibiting is considered in the following discussion.

When the scan period begins, the delay is 5%, leaving 20.0 µs between the opening of the gate (identically the beginning of the stretch time) and the end of the time base (19 µs plus an additional 1 µs of reset time --- Table III-1 shows the reset time for each time base). Because the stretch time is only 10 µs, it falls well within the time base duration, and only the first of the four holdoff or inhibit conditions applies. Thus, early in the scan period, each trigger pulse will initiate a time base. The information rate then is one sample per twenty-one microseconds.

Now consider the case when the scan has progressed to 100%. In this case the

TIME BASE DURATION	RESET TIME (TYPICAL)
2 µs	1 µs
5 µs	1 µs
10 µs	1 µs
20 µs	1 µs
50 µs	1 µs
0.1 ms	1 µs
0.2 ms	100 µs
0.5 ms	100 µs
1.0 ms	100 µs
2.0 ms	100 µs
5.0 ms	100 µs
10 ms	100 µs
20 ms	5 ms
50 ms	5 ms
100 ms	5 ms
200 ms	5 ms
500 ms	5 ms
1.0 s	5 ms
2.0 s	0.5 s
5.0 s	0.5 s
10 s	0.5 s
20 s	0.5 s

TABLE III-1. TIME BASE RESET TIMES

stretch period begins as the time base is ending, adding a 10 µs inhibition period (second inhibiting condition). As a result, instead of each trigger initiating a time base, every other trigger will initiate one, with a corresponding reduction in the information rate from one sample per twenty-one microseconds to one sample per forty-two microseconds. Thus, the information rate at the end of the scan is only half what it was in the beginning. The consequence of this anomaly is a change in the output signal-to-noise ratio over the scan period. If the scan rate had been selected according to the higher information rate, the resolved output waveform would be "blurred" toward the end of the scan. The solution to the problem in this case is select the proper combination of time base and Final Delay. If the time base were set to 50 µs and the Final Delay dial set to 44% (22 µs), the signal would be processed as rapidly as possible consistent with maintaining a constant information rate (one sample per forty-two microseconds).

Duty factor limitations can pose problems with very low repetition rates, as is explained in subsection 3.4I.

3.4E APERTURE TIME (gate width)

The aperture time (duration of the gate opening) is set by the dual-concentric Aperture Time control. The outer dial, a detented switch, selects the Aperture Time range, while the inner dial, a potentiometer, acts as a multiplier. Figure III-5 shows the control setting for an aperture time of 30 µs.

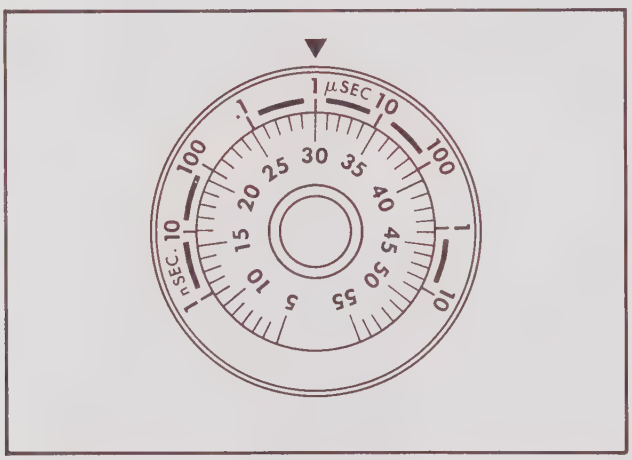


Figure III-5. APERTURE TIME CONTROL

Note that the multiplier ratio is 11:1 (55:5 on the dial symbolization), with the result that some aperture times can be set in two different ways. For example, to set an aperture time of 50 µs, one could: (1) set the range to 1 µSEC. and the multiplier to 50, or, (2) set the range to 10 µSEC. and the multiplier to 5. In principle, the two settings are equivalent, but the higher setting (multiplier to 50) will be more accurate.

In selecting aperture time, one must make a compromise between resolution, output noise-to-signal ratio, and experimental time. Although it is always

desirable to keep all three as small as possible, achieving any two of the objectives always seems to mean sacrificing the third. In the following paragraphs, these three "conflicting" objectives are discussed in detail, after which, specific procedures for operating in the high and normal resolution modes respectively are given.

RESOLUTION

The aperture time determines the basic system resolution of the Model 160. If two signals are separated in time by Δt seconds, and the aperture time is Δt seconds, the two signals will be blurred together at the output but still clearly resolvable. Another way of specifying the resolution limitation is to consider the effective rise and fall time of the Model 160 to be equal to the aperture time. Figure III-6 shows how the aperture time affects the recovery of an input pulse of duration Δt. Note that the processed waveform, in addition to showing wave shape distortion with wide apertures, undergoes an apparent time shift equal to the aperture time.

EXPERIMENT TIME

The observed time constant, also referred to as the real-time time constant, governs the response time of the instrument when operating. It equals the effective time constant (see TIME CONSTANT, 3.4H) divided by the product of the Aperture Time times the trigger repetition rate.

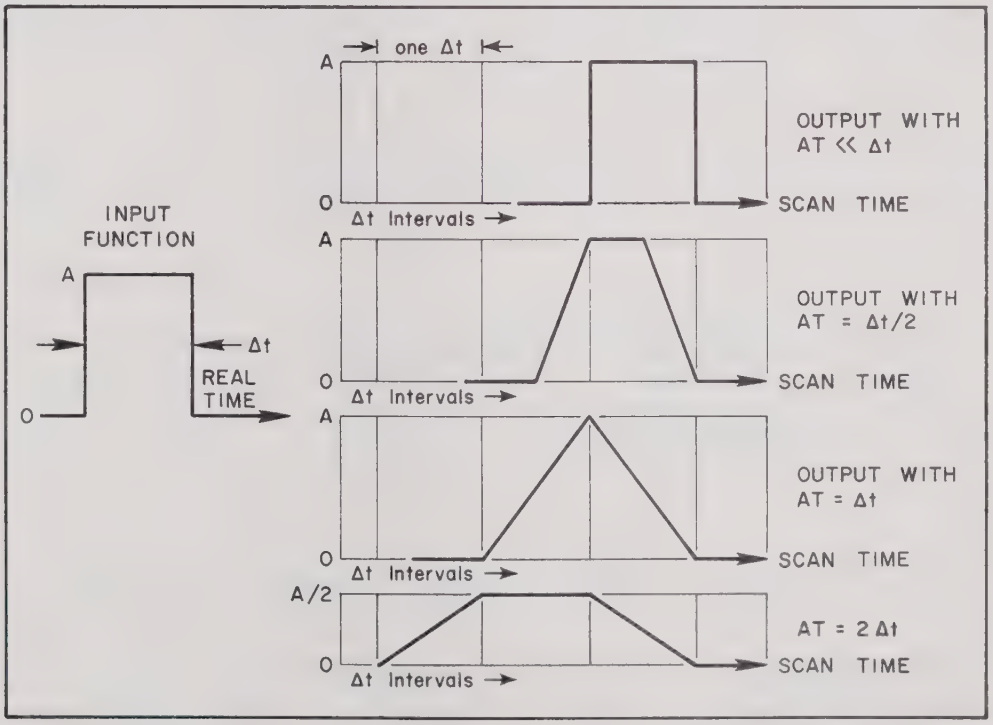


Figure III-6. RELATIVE DISTORTION OF PROCESSED PULSE AS A FUNCTION OF APERTURE TIME

For single point analysis, five times the observed time constant are required for the output to fully respond (within ½%) to the input signal over the aperture time interval. Because the observed time constant varies inversely with the aperture time, the use of aperture times smaller than absolutely necessary unduely prolongs the time required to recover the signal. In the case of scanned operation, the scan time which yields a step function response equal to that obtained by point-by-point analysis varies as the inverse square of the aperture time, making it even more important to realistically appraise the required resolution.

If fixed-point analysis is being performed, narrowing the aperture allows less information to be processed over the aperture time interval, as illustrated in the following example. Assume a full-scale input step function and a time constant of 100 ms. If the gate were continuously open, the output would respond to the step function at a rate determined solely by the time constant. As shown in Figure III-7b, the output would reach full scale in five time constants (0.5 s). Assume the selected sensitivity to be one volt. The volt-second requirement for the output to fully respond is 0.5 volt-seconds,

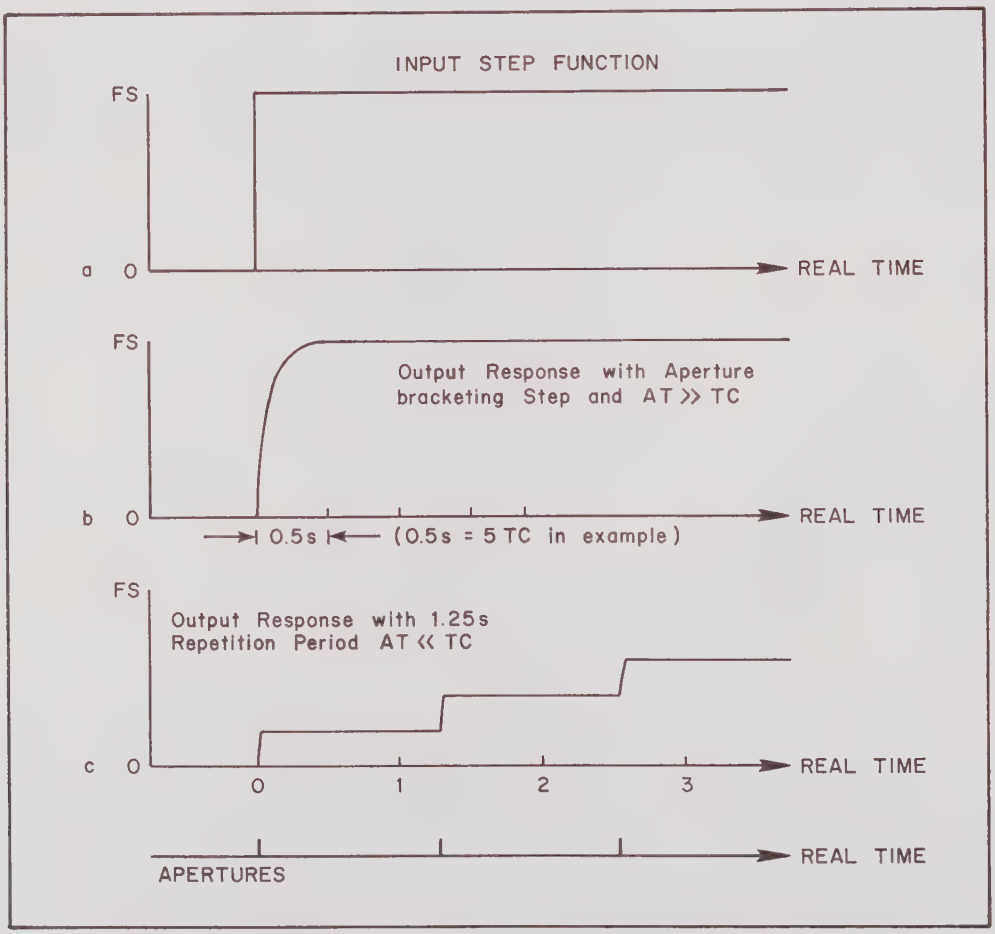


Figure III-7. EFFECT OF SAMPLING ON OUTPUT RESPONSE TIME

given by the product of the full-scale signal (one volt) times five time constants (one time constant is 100 ms). This requirement must be satisfied at all times. Hence the reason for the slowed response when sampling. Figure III-7c shows how this applies to the example under consideration. Assume that the step function is being sampled (fixed-point analysis) for 10 ms every 1.25 s. Because the same volt-second requirement must be satisfied, and the gate conducts for only 10 ms every 1.25 s, the total time required for the output to fully respond is 62.5 s (volt-second requirement of 0.5 s divided by the ratio of the aperture time to the repetition period, 10 ms/ 1.25 s). The ratio of the aperture time to the repetition period is defined as duty factor and is discussed in detail later.

SIGNAL-TO-NOISE

Assuming the output has had time to fully respond, the signal-to-noise improvement ratio (SNIR) is given by:

$$SNIR = \sqrt{\frac{2 \times \text{Time Constant}}{\text{Aperture Time}}}$$

, where both the time constant and the aperture time are given in seconds.

In the normal resolution mode, the time constant in question is that selected with the red symbolized Time Constant switch. In the high resolution mode, the time constant is the "effective" time constant (see 3.4H, TIME CONSTANT), which takes into account both time constant switches as well as the aperture time and stretch time. Consequently, it becomes more convenient to define SNIR in terms of the observed time constant, that is:

$$SNIR = \sqrt{2\ (OTC)\ f}$$

, where OTC is the observed time constant and "f" is the trigger repetition frequency. The high resolution mode observed time constant can be computed from the formulas given in Figure III-10, page III-24.

HIGH RESOLUTION MODE

When the aperture time is in the range of 10 ns to 5500 ns, the setting of the Aperture Range will be 1 nSEC, 10 nSEC, or 100 nSEC. Note that these three range settings are marked in blue to indicate that the instrument has automatically been switched into the high resolution mode, with the following attendant characteristics and restrictions.

(1) Aperture times down to 10 ns can be used.

(2) The maximum input voltage may not exceed 3.5 times full scale without causing clipping and output distortion.

(3) The Time Constant switch having the blue symbolization becomes effective. (The red-symbolized Time Constant switch is effective at all times.)

(4) For certain combinations of aperture time, time constant, and repetition rate, use of the Retention control is suggested.

The following procedure determines whether the Retention control need be adjusted and contains instructions for making the adjustment.

(1) According to the experimental requirements, set the aperture time, time base, trigger mode, time constant(s) (see subsection 3.4H), and stretch time (normally 30 μs). Then establish proper triggering.

(2) Set the Input Coupling switch to GRD, the Input Offset switch to OFF, the Retention control to OFF, and the Sensitivity switch to 10 V.

(3) Adjust the Zero control for exactly center-scale (zero) meter indication, or slightly positive (less than one percent of full scale).

(4) Set the Sensitivity switch to CAL. and note the resulting positive meter deflection. After the output has had time to fully respond, the meter indication should be full scale. If it is full scale, the Retention control need not be used. If it does not indicate full scale, adjust the Retention control as follows.

(5) Turn the Retention control on and continue turning the control clockwise as required to obtain the desired full-scale meter indication. NOTE: Retention control settings close to the OFF position yield near-zero meter indications.

(6) Set the Sensitivity switch to 10 V and re-adjust the Zero control for exactly zero on the meter.

(7) Reset the Sensitivity switch to CAL. and adjust the Retention control for exactly full-scale meter indication.

(8) Repeat steps 6 and 7 until the two end-points (zero and full scale) are exactly correct. When this is accomplished, the Retention control is properly adjusted. At that time the Sensitivity switch can be adjusted to the sensitivity appropriate to the experiment. NOTE: If, in the course of the experiment, the aperture time, time constant (blue), or repetition rate is changed, it may be necessary to readjust the Retention control as directed in this procedure.

When optimizing the setting of the Retention control, it is preferable to make the adjustment at the expected input trigger rate. However, if the input trigger rate is low, this may become difficult because of the long time required to achieve equilibrium. One solution is to temporarily speed up the trigger rate to set the retention, and then, after the retention is set, to slow it up again to the experimental trigger rate for operating. The trigger rate can be easily speeded up by transferring to the Recurrent Trigger mode and, if necessary, selecting a shorter time base, the only limitation being that the repetition period must be at least ten times longer than the selected stretch time. In the case of instruments equipped with the Analog Memory option, it is not necessary to enable the analog memory prior to setting the Retention control. This control and the memory are fully independent.

For example, if the experimental input trigger rate were 50 Hz (20 ms) and

the stretch time 100 μs, the repetition rate could be increased to 1000 Hz $(10 \times 100\ \mu s)^{-1}$ to set the Retention control.

NORMAL RESOLUTION MODE

Over the aperture time range of 0.5 s to 0.55μs the Model 160 operates in the normal resolution mode. (For those users who are familiar with the PAR™ Model CW-1, the Model 160 operating in the normal resolution mode is almost identical to the Model CW-1.) No special procedures are necessary in this mode, only those standard requirements with regard to duty factor, time constant, etc., which are discussed further on in this section.

Note that aperture times in the range of 0.5 μs to 5.5 μs can be obtained in either the high or normal resolution modes, the difference being one of dynamic range as explained in subsection 3.4M.

3.4F SCAN TIME AND RESOLUTION

As mentioned earlier, the instantaneous delay between the external trigger and the position of the gate opening is automatically increased when the instrument is operating in the scanned delay mode. The processed output, therefore, is a replica of the averaged real time waveform slowed down by the scan rate. Thus the waveform can be recorded by means of an X-Y plotter or storage oscilloscope for further analysis.

Selecting the proper scan rate is critically important because it directly affects the resolution. To obtain a resolution equal to the selected aperture time, the scan must progress no faster than one aperture time width per five times the observed time constant (observed time constant equals time constant divided by the duty factor). Use of faster scan rates results in loss of resolution. Use of slower scan rates is wasteful of experiment time and results in little improvement in resolution. The following formula relates the minimum scan rate (MSR) to the other operating parameters.

$$\text{MSR (minutes)} = \frac{\text{(Time Constant) x (Time Base)}}{12 \times \text{(Repetition Rate) x (Aperture Time)}^2}, \text{ with all}$$

parameters expressed in seconds. In the normal resolution mode, the time constant in question is that selected with the red symbolized Time Constant switch. In the high resolution mode, the time constant is the "effective" time constant (see 3.4H, TIME CONSTANT), which takes into account both time constant switches as well as the aperture time and stretch time. Consequently, it becomes more convenient to define MSR in terms of the observed time constant, that is:

$$\text{MSR} = \frac{\text{TB} \times \text{OTC}}{\text{AT} \times 12} \text{ minutes.}$$

The high resolution mode observed time constant can be computed from the formulas given in Figure III-10, page III-24.

Be sure that the repetition rate is the true one, that is, the number of time base ramps or gate openings per second as opposed to the number of input triggers per second, which can be a higher number.

Consider the following high-resolution mode example. Assume the selected time base is 2 ms, the aperture time is 100 ns, and the repetition frequency is 100 repetitions per second. Further suppose that the red symbolized Time Constant switch is set to .01 ms, while the blue symbolized Time Constant switch is set to 3 μs. The stretch time shall be assumed to be 100 μs. Using the high resolution mode observed time constant formula (Figure III-10, page III-24), one obtains an observed time constant of 0.3 s. Putting this number and the other parameters into the high resolution MSR formula, one obtains:

$$MSR = \frac{2 \times 10^{-3} \times 3 \times 10^{-1}}{10^{-7} \times 12} = 500 \text{ minutes.}$$

Note that the experiment time need not necessarily be 500 minutes, but that the rate at which the aperture is scanned through the time base be 500 minutes per 100% of time base. If the desired waveform appeared over only 5% of the time base, the total process time would be reduced to 25 minutes.

One might use the following procedure to recover a waveform when operating in the scanned delay mode.

(1) Establish proper triggering.

(2) Select the time base according to the considerations in subsection 3.4C.

(3) Select SCAN with the Delay Mode switch.

(4) Establish and set the appropriate aperture time, time constant, stretch time, and retention.

(5) Set the Single/Repeat switch to the desired position.

(6) Establish the two scan limits, that is, the setting of the Initial Delay and Final Delay dials.

(7) Depress the Scan Reset pushbutton.

(8) Release the Scan Reset pushbutton when convenient and record.

The Model 160 will then scan the time base period from the initial to the final delay limits. If the Single/Repeat switch is set to SINGLE, one scan only will occur, after which the Tilt light will come on. If the switch is set to REPEAT, successive scans over the set limits will take place. This scanning will continue indefinitely.

HOLD

During the course of a scan, it may be desirable to stop the scan and examine some fine detail. This is conveniently accomplished by transferring the Scan Mode switch from SCAN to HOLD when the scan has reached the point of interest. At that time the delay will "hold" at the value just attained. The Initial Delay dial can be used to vary the delay about the attained value. If one desires to resume scanning, return the Initial Delay dial to its original setting and return the Delay Mode switch to the SCAN position. The scan will then continue as usual.

SCAN-RATE CHANGE

It may be advantageous to change the scan rate during the course of an analysis. This is especially true if a "survey run" is being conducted where the character of the waveform is not well known in advance. Where this is the case, one should try a relatively fast scan first. If the results of this trial scan indicate the presence of relevant information, reduce the scan rate as required to satisfy resolution criteria.

EXTERNAL SCAN/DELAY

Certain experimental situations may call for perfect correlation of the delay scan with a physical parameter, such as magnetic field. This can be accomplished by applying the appropriate zero-to-10 V (positive dc) level to the rear-panel Scan Delay External Input jack (input resistance of approximately 3 kΩ). The following steps are suggested to establish operation in this mode.

(1) Set the Final Delay dial to 100%.

(2) Set the Scan Rate switch to EXT.

(3) Apply the appropriate delay voltage to the rear-panel External Delay jack.

3.4G DUTY FACTOR LIMIT

INTRODUCTION

During each time base period the Model 160 averages over the aperture time interval only. For all of the time between aperture pulses, the output of the instrument is expected to "hold" at the level reached during the previous aperture pulse. It is this ability to hold (or lack thereof) which directly determines how small the duty factor (ratio of aperture time to repetition period) can be without adversely affecting the accuracy of the instrument. Although the hold characteristics of the Model 160 are quite good, leakage currents do exist which impose limits on the allowable duty factor. These limits are separately considered for normal and high resolution operation.

NORMAL RESOLUTION MODE

The duty factor limit for the Model 160 is a function of time constant as shown in Figure III-9. It is defined as that duty factor for which the output may change as much as ±1% of full scale between aperture pulses. Note that Figure III-9 contains three curves. The solid line shows the duty factor limit as a function of time constant, where the time constant is that selected by the red symbolized Time Constant switch. With a time constant of 10^{-5} s (.01 mSEC), the duty factor limit is 10^{-6}, the best obtainable with the Model 160. Over the range of 10^{-4} s to 10^{-1} s, the duty factor limit is a constant 10^{-5}. With higher time constants, the duty factor limit degrades steadily, reaching 10^{-2} with a 100 second time constant. For small time constants (10^{-5} s to 10^{-1} s), the duty factor limit is largely the result of sampling gate leakage currents. For time constants of 0.3 s and longer, the duty factor limit results from leakage currents through the integrating capacitor.

The dashed line (Figure III-9) shows the duty factor limit obtainable when using external capacitors and operating with the Time Constant switch set to .01 mSEC. This means of operating allows the best duty factor limit (10^{-6}) to be extended to a time constant of 10^{-2} s. The time constant value depends on the size of the external capacitance as shown in Figure III-9. These external capacitors should be connected between pins P and R of the rear-panel interface connector. External time constant capacitors must be of a low leakage, high quality dialectric material type, such as Mylar*, Polycarbonate, or Polystyrene. Preferably, they should be individually selected for insulation resistances of at least 10^{12} ohms. Note that there is no advantage in using external time constant capacitors to obtain time constants of 10^{-1} or longer.

The dotted line in Figure III-9 shows the improvement in duty factor limit attainable by using the analog storage accessory (optional). This improvement is read from the scale at the right of the figure. Note that, with time constants longer than 10^{-1} s, there is no advantage to be obtained by using the analog storage accessory. However, with smaller time constants, the improvement factor increases linearly, reaching a maximum of 200 with a time constant of 10^{-4} s.

The Observed Time Constant (red symbolized TC divided by product of AT times repetition frequency) is the real time required for the processed output signal to reach 63% of its true eventual value. Figure III-8 shows the residual error as a function of elapsed time, where elapsed time is normalized in units of OTC (Observed Time Constant), and where residual error, as a percentage of the final output level, is defined as the difference between the output level at any time, and the final output level. Note that the output reaches within 1% of its final value after 4.6 OTC.

ANALOG STORAGE ACCESSORY (Normal Resolution Mode)

In some applications, the duty factory limit may be appreciably increased by

*DuPont Registered Trademark.

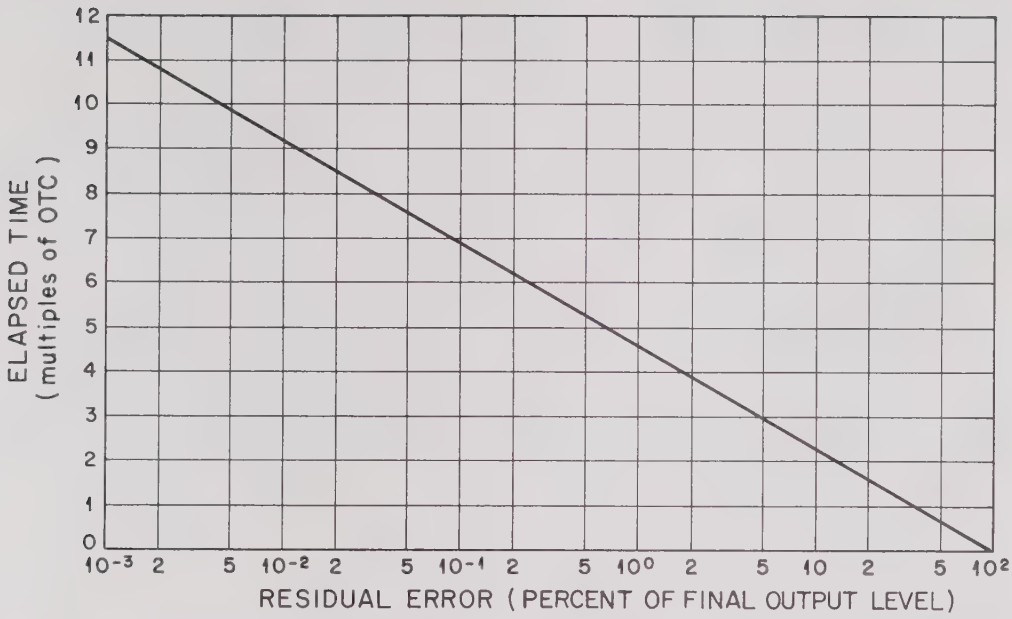


Figure III-8. RESIDUAL ERROR VERSUS ELAPSED TIME

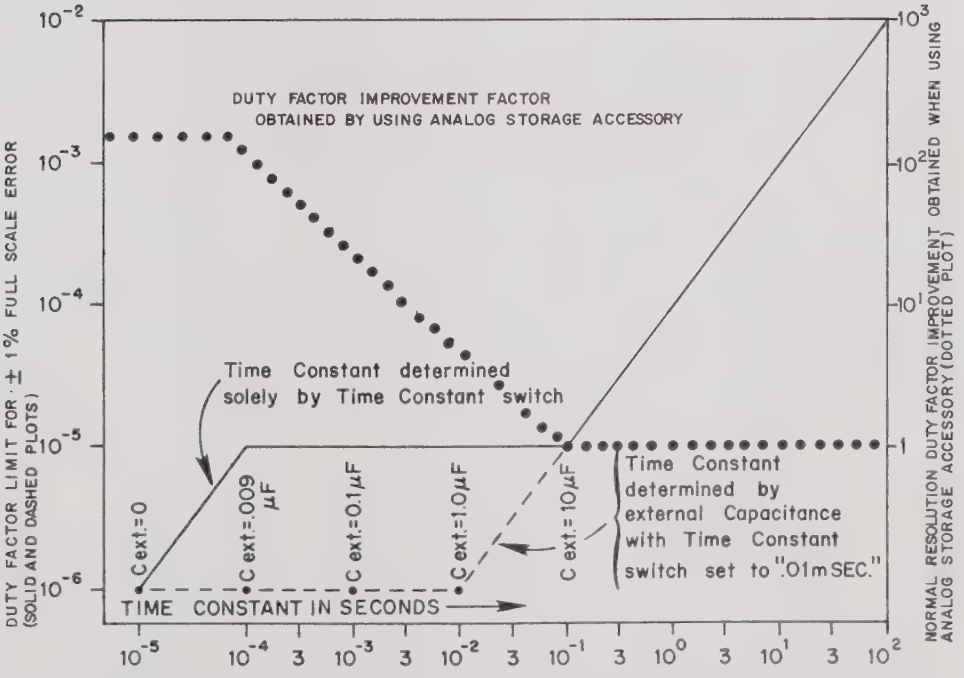


Figure III-9. DUTY FACTOR LIMIT AS A FUNCTION OF TIME CONSTANT

using the optional Analog Storage accessory. If the trigger repetition rate is 100 Hz or less, and the time constant is less than 100 ms, the duty factor limit may be increased by as much as a factor of 200, as shown in Figure III-9.

To energize the analog storage accessory, one need only set the Memory switch to ON. The associated indicator lamp will light, indicating that the Analog Storage facility is active. The memory can only be activated when operating in the External Trigger Mode. It is automatically inhibited in both the Recurrent and Continuous Gate modes.

The chief utility of the Analog Storage accessory is that it allows one to have the long holding times associated with the longer time constants, while realizing the rapid acquisition and analysis obtainable by operating with a short time constant. However, for very short normal resolution aperture times (approaching one microsecond), the effective or observed time constant may be somewhat increased due to the finite time (approximately 0.1 μs) required to internally switch between the "process" and "store" conditions. This same switching time transition may also cause a small but noticeable offset when the Analog Storage accessory is activated. The offset may be compensated by adjusting the front-panel Zero control.

HIGH RESOLUTION MODE

When operating in the high resolution mode, the normal resolution mode circuits are used to hold or stretch the output of the fast sampler. With the setting of the Retention control optimized, the high resolution mode duty factor limit is a function of the normal (red symbolization switch) time constant and the ratio of the aperture time to the stretch time. Consider the following example. Suppose one is operating with a time constant of 0.1 ms (the setting of the high-resolution time constant is immaterial), a stretch time of 10 μs, and an aperture time of 0.2 μs. To compute the high-resolution duty factor limit, first compute the normal-resolution duty factor limit. From Figure III-9, the duty factor limit with a time constant of 0.1 ms is 10^{-5}. This number is then multiplied by the ratio of the aperture time to the stretch time to compute the duty factor limit. After multiplying the "normal" duty factor limit (10^{-5}) by the ratio (2×10^{-2}), one obtains as the duty factor limit in this example, (2×10^{-7}). In effect, the duty factor limit is improved by the ratio of the stretch time to the aperture time. There is, however, an upper limit to the attainable improvement, that limit being approximately a factor of 1000. Expressed mathematically:

$$\text{HR DUTY FACTOR LIMIT} = \text{NR DUTY FACTOR LIMIT} \times \frac{AT}{ST}$$

$$\text{for } \frac{ST}{AT} \leqq 10^3,$$

where AT is the aperture time and ST is the stretch time, both in seconds.

ANALOG STORAGE ACCESSORY (High Resolution Mode)

As mentioned in the preceding discussion, the duty factor limit when operating in the high resolution mode can be improved by as much as a factor of 1000 over what it is in the normal resolution mode by selecting the appro-

priate stretch time to aperture time ratio. If the Analog Storage accessory is used as well, an additional improvement in duty factor limit can be obtained, up to a factor of 200 as indicated in Figure III-9.

3.4H TIME CONSTANT

INTRODUCTION

The choice of time constant is particularly important in obtaining good experimental results because of the many different parameters it affects. First, and most important, the time constant, along with the aperture time, determines the improvement in signal-to-noise ratio. Second, the time constant is one of the key factors affecting the time required to recover a point or entire waveform. Third, the time constant influences the amount of internal noise which will appear at the output. Fourth, the time constant affects the duty factor limit and the "hold time" or memory drift.

NORMAL RESOLUTION MODE

When operating in the normal resolution mode, the time constant is determined solely by the setting of the normal Time Constant switch (red symbolization), which allows time constants from 0.01 s to 100 s to be selected. By connecting an external capacitor between pins P and R of the rear-panel Interface connector, one can obtain a time constant longer than that indicated by the switch position. The time constant obtained is given by the formula:

Time Constant $\cong$ 10 R_e (C_e + C_{ext}), where R_e and C_e are the equivalent R's and C's given in Table III-2, and C_{ext} is the capacitance of the external capacitor.

Selected Time Constant	R equivalent	C equivalent
.01 mSEC.	1.0 kΩ	.001 µF
.1 mSEC.	8.5 kΩ	.001 µF
.3 mSEC.	8.5 kΩ	.003 µF
1 mSEC.	8.5 kΩ	.012 µF
3 mSEC.	8.5 kΩ	.03 µF
10 mSEC.	8.5 kΩ	.12 µF
30 mSEC.	8.5 kΩ	.33 µF
100 mSEC.	8.5 kΩ	1.2 µF
.3 SEC.	8.5 kΩ	3.3 µF
1 SEC.	8.5 kΩ	12 µF
3 SEC.	14 kΩ	20 µF
10 SEC.	46 kΩ	20 µF
30 SEC.	135 kΩ	20 µF
100 SEC.	422 kΩ	20 µF

Table III-2. EQUIVALENT RESISTANCE AND CAPACITANCE AS A FUNCTION OF SELECTED TIME CONSTANT

RELATED PARAMETER	GENERAL CASE	CASE FOR $\frac{TC]_{NR}}{ST} << \frac{TC]_{HR}}{AT}$	CASE FOR $\frac{TC]_{NR}}{ST} >> \frac{TC]_{HR}}{AT}$
	CONTROL SETTINGS ASSUMED FOR EXAMPLES BELOW $TC]_{HR}$ = 1 μSEC. $TC]_{NR}$ = 1 mSEC. AT = 50 nSEC. ST = 100 μSEC. f = 1 kHz TB = 10 μSEC.	CONTROL SETTINGS ASSUMED FOR EXAMPLES BELOW $TC]_{HR}$ = 1 μSEC. $TC]_{NR}$ = .01 mSEC. AT = 50 μSEC. ST = 100 μSEC. f = 1 kHz TB = 10 μSEC.	CONTROL SETTINGS ASSUMED FOR EXAMPLES BELOW $TC]_{HR}$ = 1 μSEC. $TC]_{NR}$ = 10 mSEC. AT = 50 nSEC. ST = 100 μSEC. f = 1 kHz TB = 10 μSEC.
OTC (Observed Time Constant)	FORMULA $OTC \simeq \left(\frac{1}{f}\right)\sqrt{\left(\frac{TC]_{HR}}{AT}\right)^2 + \left(\frac{TC]_{HR}}{ST}\right)^2}$ EXAMPLE $OTC \simeq \frac{1}{10^3}\sqrt{\left(\frac{10^{-6}}{5X10^{-8}}\right)^2 + \left(\frac{10^{-3}}{10^{-4}}\right)^2} \simeq .022\ s$	FORMULA $OTC \simeq \left(\frac{1}{f}\right)\left(\frac{TC]_{HR}}{AT}\right)$ EXAMPLE $OTC \simeq \frac{1}{10^3}\left(\frac{10^{-6}}{5X10^{-8}}\right) \simeq .02\ s$	FORMULA $OTC \simeq \left(\frac{1}{f}\right)\left(\frac{TC]_{NR}}{ST}\right)$ EXAMPLE $OTC \simeq \frac{1}{10^3}\left(\frac{10^{-2}}{10^{-4}}\right) \simeq .1\ s$
SNIR (Signal—to—Noise Improvement Ratio)	FORMULA $SNIR = \sqrt{2\,(OTC)f}$ $\simeq \left[2\sqrt{\left(\frac{TC]_{HR}}{AT}\right)^2+\left(\frac{TC]_{NR}}{ST}\right)^2}\right]^{1/2}$ EXAMPLE $SNIR \simeq \sqrt{2X2.2X10^{-2}X10^{3}}^{*} \simeq 6.6$	FORMULA $SNIR = \sqrt{2(OTC)f} \simeq \sqrt{\frac{2\,TC]_{HR}}{AT}}$ EXAMPLE $SNIR \simeq \sqrt{\frac{2X10^{-6}}{5X10^{-8}}}^{*} \simeq 6.3$	FORMULA $SNIR = \sqrt{2(OTC)f} \simeq \sqrt{\frac{2\,TC]_{NR}}{ST}}$ EXAMPLE $SNIR \simeq \sqrt{\frac{2X10^{-2}}{10^{-4}}}^{*} \simeq 14.1$
MSR (Minimum Scan Rate)	FORMULA $MSR = \left(\frac{TB}{AT}\right)\left(\frac{OTC}{12}\right)$ minutes EXAMPLE $MSR \simeq \left(\frac{10^{-5}}{5X10^{-8}}\right)\left(\frac{2.2X10^{-2}}{1.2X10^{1}}\right)^{*} \simeq .37$ minutes $\therefore$ USE ONE MINUTE SCAN TIME. * Value for OTC taken from above computation.	FORMULA $MSR = \left(\frac{TB}{AT}\right)\left(\frac{OTC}{12}\right) \simeq \frac{(TB)\,(TC]_{HR})}{12(AT)^2\,(f)}$ minutes EXAMPLE $MSR \simeq \left(\frac{10^{-5}}{5X10^{-8}}\right)\left(\frac{2X10^{-2}}{1.2X10^{1}}\right)^{*} \simeq .33$ minutes $\therefore$ USE ONE MINUTE SCAN TIME.	FORMULA $MSR = \left(\frac{TB}{AT}\right)\left(\frac{OTC}{12}\right) \simeq \frac{(TB)\,(TC]_{NR})}{12(AT)(ST)f}$ EXAMPLE $MSR \simeq \left(\frac{10^{-5}}{5X10^{-8}}\right)\left(\frac{10^{-1}}{1.2X10^{1}}\right)^{*} \simeq 1.67$ minutes $\therefore$ USE TWO MINUTE SCAN TIME.

ABBREVIATIONS

$TC]_{HR}$ — Setting of blue symbolized Time Constant Switch.
$TC]_{NR}$ — Setting of red symbolized Time Constant Switch.
f — Trigger repetition frequency.
AT — Selected Aperture Time.
ST — Selected Stretch Time.
TB — Time Base Duration.

Figure III-10. TIME CONSTANT AFFECTED PARAMETERS IN HIGH RESOLUTION MODE

The observed time constant (OTC) is the time required for the output to reach 63% of its final value. When operating in the normal resolution mode, it is a simple function of the red-symbolized Time Constant switch setting, the aperture time, and the repetition frequency, the formula being:

$$OTC = \left[\frac{TC}{AT}\right]\frac{1}{f}$$

In other words, the observed time constant equals the selected time constant divided by the duty factor.

HIGH RESOLUTION MODE

When the instrument is switched into the high resolution mode, the blue symbolized Time Constant switch becomes effective. However, the red symbolized switch also remains effective, complicating the problem of determining the actual time constant. Consequently, when operating in the high resolution mode, one must think in terms of an "effective" time constant which takes into account the setting of both Time Constant switches as well as other parameters. In other words, in the high resolution mode, the observed time constant (OTC), the improvement in signal-to-noise ratio, and all other time constant affected factors, are related to the "effective" time constant in the same manner as they are related to the setting of the red symbolized Time Constant switch when operating in the normal resolution mode.

As shown in Figure III-10, the OTC can be computed directly from the control settings and operating conditions. Note that the relative size of the normal (red) resolution time constant to stretch time ratio and high resolution (blue) time constant to aperture time (blue) ratio is the critical relationship in determining OTC, and hence the effective time constant, which is simply given by:

$$TC\ effective = OTC \times AT \times f$$

In most instances, it is more convenient to think in terms of the observed time constant (OTC). Unlike the normal resolution mode, where the observed time constant is simply the selected time constant divided by the product of the aperture time times the repetition frequency, the high resolution mode OTC is a somewhat complicated function of the two time constant settings, the aperture time, the stretch time, and the repetition frequency. Figure III-10 gives the general case formula for OTC in the high resolution mode, and shows how it can be used to determine SNIR and MSR in the high resolution mode. Also given are analogous examples for the two limiting cases. In the first case, the normal resolution time constant to stretch time ratio is much smaller than the high resolution time constant to aperture time ratio. In the second, the reverse is true. Operating under "second limiting case conditions" can be particularly advantageous in certain situations. For example, in the case of very noisy signals, it allows far higher time constants to be achieved than can be achieved by means of the blue symbolized Time Constant switch alone. Another advantage emerges when one is operating with the retention active. This results from the necessity of having to reset the Retention control if the setting of the "fast" Time Constant switch is changed. However, changing the time constant by means of the normal resolution Time Constant switch only does not have any effect on the required retention.

As previously mentioned, the high resolution effective time constant is computed by multiplying the OTC, as determined from Figure III-10, by the product of AT x f. Note that the resulting expression is simple for the two limiting cases. In the first limiting case, where the normal resolution time constant to stretch time ratio is much smaller than the high resolution time constant to aperture time ratio, the effective time constant is simply the time constant selected by the blue symbolized time constant switch. For the second limiting case, where the normal resolution time constant to stretch time ratio is much larger than the high resolution time constant to aperture time ratio, the effective time constant is:

$$\text{TC effective} = \frac{TC]_{NR} \times AT}{ST}$$

It should be mentioned that the general case formula given in Figure III-10 is only an approximation. However, the accuracy of the OTC computed with this formula, and with the limiting case formulas, is certainly accurate enough for the purpose at hand, namely, to allow the Model 160 controls to be properly set for optimum operation.

SIGNAL-TO-NOISE IMPROVEMENT RATIO

The Model 160 improves the signal-to-noise ratio by means of a sampling and averaging technique. At any time, the voltage at the output is the average of some previous number or samples, and, if the output has had time to fully respond (five time constants of sampling time, or, in terms of real time, five times the observed time constant), that number of samples will be very nearly two times the time constant divided by the aperture time. Clearly, the larger this number, the more nearly the noise about the sampled point will average to zero, and the greater will be the improvement in voltage signal-to-noise ratio. From a consideration of the number of samples averaged, a Signal-to-Noise Improvement Ratio (SNIR) may be defined as:

$$\text{SNIR} = \sqrt{\frac{2 \times \text{Time Constant (sec.)}}{\text{Aperture Time (sec.)}}}$$

Example: TC = 100 μs
AT = 1 μs
SNIR = $\sqrt{200} \simeq 14$

In the normal resolution mode, the time constant in question is that selected with the red symbolized Time Constant switch. In the high resolution mode, the time constant is the "effective" time constant discussed previously. Consequently, it is more convenient to define SNIR in terms of the OTC, that is:

SNIR = $\sqrt{2(OTC)f}$, where OTC is the observed time constant as computed from the formulas given in Figure III-10, and "f" is the repetition frequency.

The same degree of noise rejection may be obtained when scanning if the scan rate is determined as directed in subsection 3.4F (page III-17).

If the time constant is very large and the aperture time very narrow, or, if the input signal is not very noisy to begin with, one can improve the signal-to-noise ratio to the point where the internal noise of the instrument is dominant at the output. As a rule, however, this point usually coincides with duty factor limitations and those problems associated with extremely protracted experimental times. With long experimental times, one assumes the risk of incorporating long term drifts, physical or instrumental, into the "real" signal. Adequate performance is generally attained by simply increasing the time constant until the output "bounce" is reduced to an arbitrarily acceptable level.

When doing single point analysis with a long time constant, one can save considerable time by beginning the analysis with a small time constant, and then increasing the time constant as the output approaches its final level.

An alternative method of improving signal-to-noise is to not allow the output to reach its final value. By taking the reading well before the final level is reached, one performs a close approximation to true integration. If the aperture time is small compared to the time constant, each new sample will contribute a nearly constant volt-second piece of information to the output, and the SNIR simplifies to:

$$\text{SNIR} \simeq \sqrt{N}, \text{ where N is the number of samples in any given time}$$

interval. Assuming the output is allowed to reach no more than 40% of the final value, N is given to an accuracy of two percent by:

$$N = \frac{\text{Output Voltage at Measurement Time x Time Constant}}{\text{Aperture Time}}$$

In the normal resolution mode, the time constant in question is that selected with the red symbolized Time Constant switch. In the high resolution mode, the time constant is the "effective" time constant, making it more convenient to compute "N" in terms of the observed time constant, where the observed time constant is computed from one of the formulas given in Figure III-10. The formula then for "N" becomes:

$$N = \text{Output Voltage at Measurement Time x OTC x f}$$

This technique yields an SNIR equal to that obtainable by the normal method in about 40% of the time required in using the normal method. However, it is generally more difficult to implement because the number of integrated samples must be held absolutely fixed from one experiment to the next.

Example: An experiment produces 1 V (averaged over the experimental interval), 1 μs wide pulses at a repetition rate of 100 Hz. The experiment is such that only 200 repetitions can take place before the physical effect deteriorates sufficiently to invalidate the results. Assume an aperture time of 1 μs, a time constant of 1 ms, and a full-scale sensitivity of 1 V.

Placing these numbers in the preceding formula and solving for the Output Voltage after 200 samples, one obtains:

$$E_{out} = \frac{N \times AT}{TC} = \frac{200 \times 10^{-6}}{1 \times 10^{-3}} = 0.2 \text{ V}$$

Because this number is smaller than the 40% of full scale constraint for "true integration" analysis, the formula is valid, and the signal-to-noise improvement ratio is simply:

$$SNIR = \sqrt{200} \simeq 14$$

Assume the same signal is recovered by the conventional technique, that of allowing the output to reach its final value, in this case one volt. Because the total experimental time is limited to two seconds (200 repetitions at a repetition rate of 100 Hz), one must choose that time constant which will yield an observed time constant of two fifths of a second. In other words, in order for the output to fully respond, five times the observed time constant must elapse in two seconds. As the observed time constant equals the time constant divided by the duty factor, one can easily solve for the time constant, in this case:

$$TC = OTC \times \text{Duty Factor} = 0.4 \times AT \times f = 40 \ \mu s$$

With this time constant the SNIR will be:

$$SNIR = \sqrt{\frac{2 \times 40 \times 10^{-6}}{10^{-6}}} \simeq 9$$

Thus, by using the "pseudo" integration technique, a significantly higher SNIR was obtained than was obtained by using the conventional method.

3.4I HOLDING TIME

NORMAL RESOLUTION MODE

As mentioned in subsection 3.4G, the duty factor limit results primarily from the small but finite changes at the integrator output during the interval between samples. In the normal resolution mode, with a time constant of 10 ms or smaller, this holding time limitation is due to integrator offset current and gate leakage current. Because the output voltage change for a given input current varies inversely with the feedback capacitance of the integrator, the memory drift is given by:

$$\text{Memory Drift (volts/second)} = \frac{\text{Integrator Input Current}}{\text{Integrator Feedback Capacitance}}$$

The net input current with the gate closed is typically in the range of ±5 pA, allowing the maximum memory drift to be simplified to:

$$\text{Memory Drift (volts/second)} = \frac{5 \times 10^{-12}}{C}$$, where C is the feedback capacitance in farads. This number is an order of magnitude smaller than the

memory drift as a percentage of full scale (divide by ten because full-scale output is 10 V, and multiply by 100 to convert to percentage). Table III-3 gives the memory drift in percent per second of full scale for each position of the Time Constant switch. Note that the memory drift does not improve for time constants longer than 10 ms. Above 10 ms, the leakage current of the feedback capacitor becomes larger than the gate leakage and offset current. This leakage current is proportional to the capacitance itself, thereby limiting any further improvement in the memory drift characteristic.

If external capacitors are used, the feedback capacitance is the sum of the external capacitance and that corresponding to the selected time constant. If the external capacitor is other than a high-quality, low-leakage type, the memory drift will be severely degraded.

If an experiment is conducted with a time constant of 3 ms or smaller, the final value reached can be held longer by switching to one of the higher time constant settings (10 ms or higher) after completion of the experiment.

HIGH RESOLUTION MODE

If the Retention control is not properly adjusted, the hold time in the high resolution mode is considerably poorer than in the normal resolution mode.

With the Retention control properly set, the fast sampler need only "hold" for the duration of the stretch time (10, 30, or 100 μs). After the stretch time interval, the retention feedback signal from the "normal" integrator to the fast integrator causes the fast integrator to "retain" the previously averaged sample. Even if the Retention control is turned off, good averaging with reasonable repetition rates is achievable with the longer high resolu-

Time Constant	Feedback Capacitance	Drift (% of FS/s)
.01 mSEC.	.001 μF	.05%
.1 mSEC.	.001 μF	.05%
.3 mSEC.	.003 μF	.02%
1 mSEC.	.012 μF	.005%
3 mSEC.	.03 μF	.002%
10 mSEC.	.12 μF	.001%
30 mSEC.	.33 μF	.001%
100 mSEC.	1.2 μF	.001%
.3 SEC.	3.3 μF	.001%
1 SEC.	12 μF	.001%
3 SEC.	20 μF	.001%
10 SEC.	20 μF	.001%
30 SEC.	20 μF	.001%
100 SEC.	20 μF	.001%

Table III-3. MEMORY DRIFT AS A FUNCTION OF TIME CONSTANT (NORMAL RESOLUTION MODE)

tion time constant settings. Table III-4, page III-30, shows the high-resolution hold time characteristics as a function of the stretch time and setting of the "fast" Time Constant switch. Also indicated is the minimum repetition rate (that which yields one percent of full scale error) for each time constant when the Retention control is set to OFF.

ANALOG STORAGE ACCESSORY

In the instrument in question is equipped with the optional analog storage accessory, the memory drift as a function of time constant can be significantly improved for normal resolution time constant settings up to 100 ms. With the analog storage accessory enabled (front-panel Memory switch to ON), the drift rate, while holding, is typically 2% per hour.

It might be mentioned that the memory accessory may introduce a slight offset when operating. To prevent this offset from affecting the accuracy of the experimental results, one should do a zero correction before connecting the input signal, but with the memory accessory operating and the instrument triggering.

3.4J STRETCH TIME

In the high resolution mode, the normal resolution mode circuits are used to hold or stretch the output of the fast sampler. Three different stretch times, 10 µs, 30 µs, and 100 µs, are provided, and the choice of stretch time can significantly affect the performance of the instrument in recovering an experimental signal. Stretch time affects the duty factor limit, hold time, and time constant.

Its effect on duty factor limit is explained in subsection 3.4G under HIGH RESOLUTION MODE. In brief, the duty factor limit with a long stretch time will be better than the duty factor limit obtained with a short stretch time, other parameters remaining constant.

The effect on time constant is discussed in subsection 3.4H under HIGH RESOLUTION MODE. The central idea of that paragraph is that when operating in the high resolution mode, the stretch time and the setting of the normal resolution Time Constant switch must both be considered in determining the "effective" time constant, which governs all time constant affected parameters in the high resolution mode. Figure III-10 gives formulas and examples.

Last, the effect on holding time is explained in subsection 3.4I under HIGH RESOLUTION TIME CONSTANT. As can be seen by referring to Table III-4, the holding time is better with a short stretch time than it is with a long one.

Thus, in selecting the stretch time, one must consider the three affected parameters and pick the stretch time most advantageous in the particular experimental situation. Usually, good results will be obtained with a stretch time of 30 µs or 100 µs, a high resolution time constant setting in the range of 1 µs to 100 µs, and a normal resolution time constant of .01 ms. In any case, these are usually good settings to begin with.

Time Constant (blue symbolization)	% Full-Scale Error With Optimum Retention			Minimum Repetition Rate If Retention Is Not Used (±2% full-scale error)
	10 µs Stretch Time	30 µs Stretch Time	100 µs Stretch Time	
3 ns	5%	15%	50%	---
10 ns	5%	15%	50%	---
30 ns	5%	15%	50%	---
100 ns	2%	5%	20%	5 kHz
300 ns	2%	5%	20%	5 kHz
1 µs	.3%	1%	3%	150 Hz
3 µs	.3%	1%	3%	150 Hz
10 µs	.3%	1%	3%	150 Hz
30 µs	<.3%	<.3%	.5%	15 Hz
100 µs	<.3%	<.3%	.5%	15 Hz
300 µs	<.3%	<.3%	<.3%	1.5 Hz
1000 µs	<.3%	<.3%	<.3%	1.5 Hz

Shaded Area Shows Recommended Operating Region

Table III-4. ERRORS DUE TO HOLDING TIME LIMITATION IN HIGH RESOLUTION MODE

3.4K INPUT SELECTOR

The choice of which input connector to use is quite simple. For those experimental situations where either a moderately high input impedance is desired or where the frequency content of the signal is under 10 MHz, use the 100 kΩ input. If the signal source impedance is higher than 100 Ω, it will be necessary to take the 50 pF shunt capacitance of the 100 kΩ input into account. Usually, if the bandwidth of the input signal is low enough to allow use of the normal resolution mode, the 100 kΩ input is suitable.

For those applications where the highest resolution is desired and where the source impedance is fifty ohms, use of the 50 Ω input is mandatory. Also, 50 ohm cables must be used to interconnect the signal source and the Model 160. Suitable cable types include RG58C/U, RG188A/U, and many others. In many situations the source impedance may be other than fifty ohms (93 Ω, 110 Ω, etc.) Where this is the case, the cable impedance should be that of the source and a series resistor should be provided at the input of the Model 160 to achieve impedance matching. The resistance of the series resistor is determined by:

$$R_{series} = Z_{source} - 50 \text{ ohms.}$$

The attenuation resulting from this resistor is given by:

$$\text{Attenuation} = \frac{R_S}{Z_{source}} .$$

For best results, the unused input connector should be grounded or at least not connected to any signal source. Once the proper input connector has been selected, move the Input Selector toggle switch towards the selected input connector to connect it to the input amplifier.

3.4L INPUT COUPLING

By means of the Coupling switch, the operator can select any one of three coupling modes, "AC", "DC". and "GRD." The AC and DC positions are true coupling modes; a signal applied to the selected input connector will be routed to the signal channel input amplifier. In the GRD. position, the input of the signal channel amplifier is disconnected from the input connector (the input connector is not shorted) and grounded. Looking into the 100 kΩ input, there is 1.0 μF in series with 10 MΩ to ground. Looking into the 50 Ω input, the input resistance is 50 ohms. This direct fifty ohms to ground is present looking into the 50 Ω input for all three coupling modes.

DC COUPLING

In the DC Coupling mode, the instrument examines both the dc and ac components of the input signal. The dc component appears at the output as an offset proportional to the input sensitivity. DC coupling is usually the preferred operating mode (as long as the offset is not large enough to cause overload or otherwise limit the dynamic range) because low frequency phenomena may be investigated. However, if dc drift at the signal source is a

consideration, especially over long analysis times, ac coupling might be preferable.

AC COUPLING

In the AC position, the signal is ac coupled to the signal channel amplifier. (The 50 Ω input is dc coupled into the instrument and then ac coupled internally.) Using ac coupling prevents input dc offsets from being included in the analysis. The frequency response is down 3 dB at about 1.6 Hz. Where it is necessary to have an even lower frequency response, an external series capacitor can be used in conjunction with dc coupling. The required coupling capacitance in microfarads is given by:

$$C = \frac{1.6}{f}\ \mu F, \text{ for the 100 k}\Omega \text{ input, and}$$

$$C = \frac{3.2 \times 10^4}{f}\ \mu F, \text{ for the 50 } \Omega \text{ input. In both cases "f" is}$$

the 3 dB down frequency. If the coupling capacitor used is an electrolytic or plastic film type, be sure to shunt it with a good quality ceramic or mica capacitor for good high-frequency response.

INPUT OFFSET

For those special but all too frequent cases where dc coupling must be used, but where a high dc input offset exists, the Input Offset controls may be used to advantage. Either a positive or negative offset of up to ten times full scale may be introduced to internally bias the input signal. The calibrated offset dial allows the operator to measure the external offset by noting the dial setting required to bring the dc offset to zero.

Another reason for using the dc offset capability instead of ac coupling is that, if the input waveform is not periodic (even though it is repetitive), an instantaneous error may arise as a function of the variation in the repetition rate due to the dc averaging properties of the input ac coupling network (or any other high-pass filter).

If no dc offset is desired, keep the Offset Polarity switch set to OFF, as there is a slight (1%-2%) offset when the offset dial is fully counterclockwise.

3.4M SENSITIVITY AND OVERLOAD

During any given experiment, two considerations determine the optimum setting of the Sensitivity switch. First, the sensitivity should be sufficiently high to yield as near full-scale output as possible. Second, the sensitivity must not be so great as to cause overload, of either the input or the output signal channel.

The first consideration comes about because of the internal noise and drift of the instrument. Because these are independent of sensitivity, in making the output signal as near full scale as possible, they will represent the

smallest possible percentage of the output signal and will effect the smallest possible degradation to it. The dominant cause of drift in the Model 160 is temperature. Typically, the temperature coefficient, referred to the output, is three millivolts or 0.03% per degree Celsius. The principal noise appearing at the output is flicker noise (5 mV peak-to-peak max.)

Overload, the second consideration, occurs when the dynamic range of either the signal input channel or the output channel is exceeded. In the case of the signal input channel, this happens when the total signal (repetitive waveform plus noise, plus dc if dc coupled) exceeds the voltage indicated by the Sensitivity switch setting by more than:

10 times in the normal resolution mode
and
3.5 times in the high resolution mode.

Should this occur, the input amplifier of the Model 160 will clip the applied signal with resultant distortion at the output. In the case of the output amplifiers, overload occurs when the output voltage exceeds full scale by about 40%.

If, at the beginning of an analysis, an oscilloscope examination of the input signal shows that the waveform of interest, although noisy, is discernable, it is relatively easy to determine its approximate amplitude and select the appropriate setting of the Sensitivity switch. If, however, the signal is so noisy as to completely mask the waveform of interest, there is no easy way to select that sensitivity range which will yield nearest to full-scale output without overload. The best one can do in such a case is to periodically check that the output does not exceed plus or minus ten volts, as will be indicated by pinning of the front-panel meter. If it does, it will be necessary to select the next lowest sensitivity and begin again. Input channel overload detection is generally no problem because of the warning provided by the Overload light. The overload light does not indicate output channel overload, such overload being indicated by the meter.

As a final consideration, the rms value of the input signal (including dc if dc coupled) should not exceed 100 volts at the 100 kΩ input. At no time should the instantaneous voltage applied to this connector exceed 200 V. The voltage limit at the 50 Ω input is 10 V rms.

3.4N DYNAMIC RANGE

The problem of dynamic range is closely associated with the problem of overload. From the preceding discussion of gain and overload, it is apparent that, when the output is full scale, the highest tolerable noise-to-signal ratio at the input is either 10:1 or 3.5:1, according to whether the normal or high resolution mode is in use. If greater noise-to-signal ratios are encountered, one need only reduce the instrument sensitivity by rotating the Sensitivity switch clockwise until no input overload occurs, as indicated by the Overload light. In so doing, one should bear in mind that the output signal will be proportionally reduced, and that the internal noise and drift will constitute a greater fraction of the output signal. The loss in output

amplitude can be made up for by increasing the recorder gain. The increased drift and noise cannot be compensated for, and ultimately determines how far one can go in trading off dynamic range for decreased sensitivity.

The dominant drift effect in the Model 160 is temperature dependent. Typically, the output will change three millivolts or 0.03% of full scale per degree Celsius. If the input sensitivity were reduced by a factor of 100 to decrease the permissible input noise-to-signal ratio to 1000 to one, the drift would be proportionally increased to three percent per degree Celsius of the output signal level (1% of full scale). Clearly, when operating with such a greatly expanded dynamic range, it is important to allow the instrument ample time to warm up (two hours) and to maintain a constant environmental temperature.

Three principal types of noise appear at the Model 160 output. The first is the earlier mentioned "flicker" noise which can be as great as 5 mV pk-pk. The second comprises chopper-frequency and 60 Hz pickup, which typically do not exceed 2 mV. The third type arises because of the slight dc shift which occurs at the output each time the gate opens. This shift lasts for the duration of the gate width interval and typically does not exceed 25 mV. All three types of noise are much smaller with large values of integrating time constant than with small values. Usually, internal noise will be negligible when operating with all but the shortest time constants. Even with the small values of time constant, the second two types of noise are of little consequence because of the slow (0.1 to 1 second) time constant of most recorders. As for the flicker noise, the high input noise-to-signal ratios which necessitate dynamic range expansion also necessitate the use of large values of time constant if the required improvement in signal-to-noise ratio is to be realized. As a result, when operating under typical expanded dynamic range conditions, the flicker noise will be quite small compared to the amplitude of the recovered signal, and compared to the amplitude of that input noise which appears at the output. Drift, on the other hand, is not a function of time constant, and will generally directly determine the quality of an "expanded" record.

Another effect which complicates expanded dynamic range operation is the dc level shift which occurs at the output when either the time constant or the aperture time is changed. Although these effects are small (typically up to 3% of full scale), scale expansion causes them to be highly noticeable. The front panel Zero control, however, may be used to reset the zero. When using the Zero control, it is often desirable to temporarily choose a smaller time constant or use the Memory Reset pushbutton to clear the Integrator (and/or analog storage).

Still another source of error results from noise and pickup which are coherent with the signal and therefore become "averaged in" with the true signal. Trigger coherent pickup emanating from outside the Model 160 is easily identified (if not easily remedied) by being alert to spurious signals being either coupled to the input via common grounds and ac power distribution systems, or magnetically induced by energy being coupled through test probes, cables, etc.

Coherent pickup within the instrument is unavoidable but small. This coher-

ent pickup is most noticeable when using the shortest aperture time settings in both the normal and high resolution modes. If only single-point analysis is being performed, the effect of the pickup may be nullified by means of the Zero control. During scanned operation, a trial run without the input signal (all settings the same as for the real run, but with the Coupling switch set to GRD.) may be used to correct the true waveform by means of a "baseline correction".

Figure III-11 plots typical dynamic range as a function of aperture time.

3.4P PRE-FILTER SWITCH

As a final aid in improving dynamic range, the input signal, prior to amplification, may be processed through a low-pass filter to reject noise components higher than the frequencies of interest. The filter is, effectively, a single section RC filter with an attenuation of 6 dB/octave above the "corner frequency".

Providing the time constant of the prefilter is no longer than one tenth the

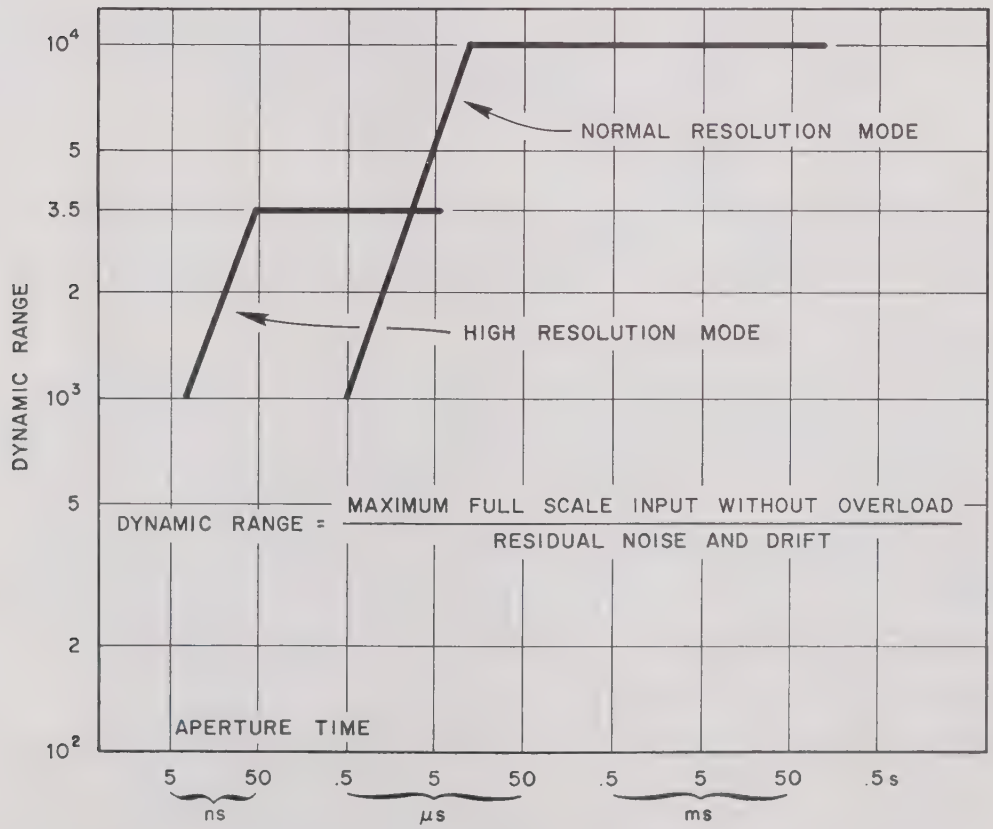


Figure III-11. TYPICAL DYNAMIC RANGE AS A FUNCTION OF APERTURE TIME

shortest integrating time constant (consistent with the resolution viz-a-viz the aperture time), there will be no loss in resolution. Prefilter time constants close to the desired resolution time will cause some "smoothing" or resolution loss. Where this is the case, the effective system rise time can be computed from:

$$t_r = \sqrt{t_p^2 + AT^2},$$

where t_r = system rise time
t_p = prefilter time constant
AT = Aperture Time

By attenuating high frequency noise, the prefilter itself achieves some improvement in signal-to-noise ratio prior to the signal averaging process. This SNIR due to the prefilter is given by:

$$SNIR = \sqrt{\frac{fin}{f_p}},$$

where f_{in} = input frequency bandwidth
f_p = prefilter bandwidth

Example: A 100 μs pulse is to be recovered by single-point analysis. The input bandwidth is assumed to be 30 MHz and the noise is assumed to be purely random. A prefilter time constant of 50 μs (3 MHz) is selected. The SNIR due to the prefilter is:

$$SNIR = \sqrt{\frac{30\ MHz}{3\ MHz}} \simeq 3.3$$

The OFF position of the Prefilter switch passes all frequencies to the amplifier, which has a bandwidth of approximately 50 MHz.

3.4Q TRANSIENT SIGNAL FIDELITY

Many applications for the Model 160 Boxcar Integrator require processing a transient signal with the highest possible fidelity. It is difficult (if not impossible) to adequately reproduce a signal whose "shape" must be determined to better than ±1%. If such experimental situations do arise where overall curve shape must be held to better than ±1%, the user should first "characterize" the signal processing instrumentation by testing with known signals and determining in advance any "aberrations" which may exist. Any resulting departures from the ideal case may then be compensated in the final calculations.

A series of suggestions for achieving best "fidelity" follows.

(1) The best high frequency response is obtained when using the "50 mV" position of the Sensitivity switch. The frequency response, and therefore the transient response, becomes poorer for the lower sensitivity positions. Figure III-12 shows the typical resolving capabilities as a function of Sensitivity switch setting.

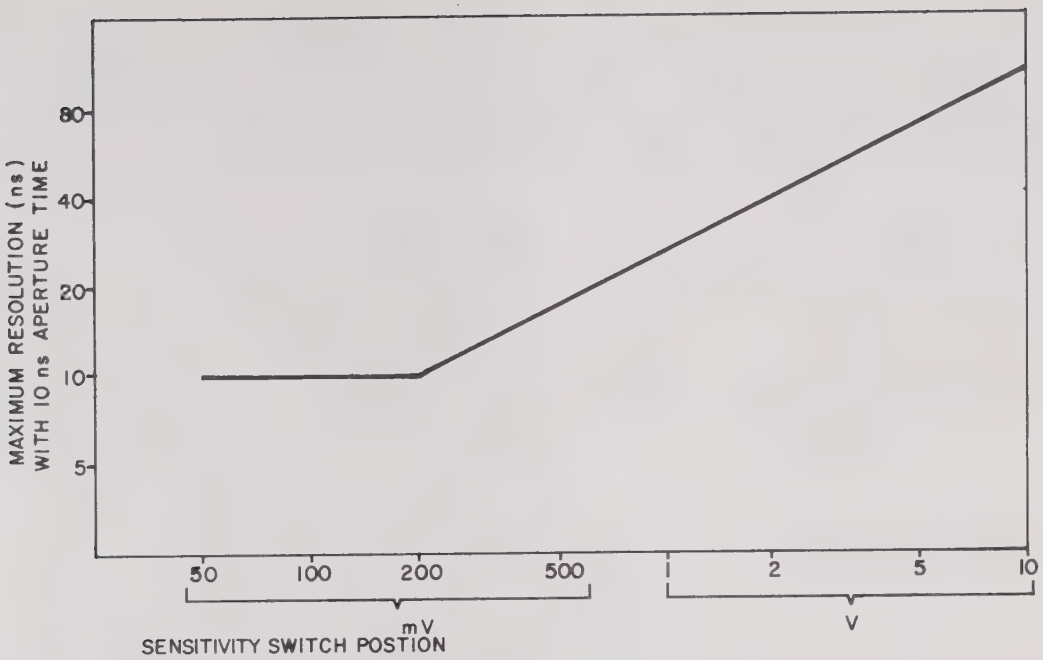


Figure III-12. RESOLUTION AS A FUNCTION OF SENSITIVITY SWITCH POSITION

To achieve additional signal attenuation while maintaining the best time resolution, use an external 50 ohm attenuator. Such attenuators are readily available in both fixed and variable attenuation versions from many manufacturers.

(2) The transient characteristics of the system may be adjusted to match the desired response by intentionally re-adjusting the compensation networks on both the Sensitivity switch and Preamplifier (see subsection 5.6). However, such a procedure is discouraged because the internal adjustment are often not returned to their original settings upon completion of the experiment.

(3) A common problem in recovering signals buried in noise is that the initial synchronizing trigger may be coupled into the signal channel, producing a spurious signal. Occasionally, this signal may be of sufficient magnitude to overload the preamplifier and subsequent circuitry, causing a rather long recovery time. Unfortunately, there is no generally recommended "cure" for this problem, but several approaches may be recommended by the PAR™ Applications Engineering staff as appropriate to the particular problem.

3.5 REAR-PANEL INPUT/OUTPUT CONNECTORS

This section of the manual discusses the purpose and applications of the rear panel connectors.

INTERFACE CONNECTOR

This connector is used to power external preamplifiers and/or to provide a single location for several key input/output points. The mating connector is a Winchester type MRE-14P-JTCH8 or equivalent.

PIN	DESCRIPTION
A	Ground Reference (power and signal)
B	+24 V at 50 mA
C	-24 V at 50 mA
D	+4.5 V at 50 mA
E	+12 V at 50 mA
F	-12 V at 50 mA
H	+ dc output (normal dc output) at 1000 ohms
K	Scan Output
J*	-200 V at 0.5 mA
M	No connection
P	External Time Constant Capacitor (integrator output)
R	External Time Constant Capacitor (integrator summing junction)

Table III-5. REAR-PANEL INTERFACE CONNECTOR

NORMAL OUTPUT

±10 V at 1000 ohms --- Tracks front-panel output.

INVERTED OUTPUT

∓10 V at 1000 ohms --- Provides same magnitude signal as the normal output but reversed in sign.

RECORDER OUTPUT

±1.3 mA for full-scale input --- Used to drive galvanometric recorders.

RECORDER OUTPUT ADJUST

Adjusts or scales current output from Recorder jack from ±0.5 mA to ±1.3 mA full scale.

EXTERNAL GATE

When the toggle switch associated with this connector is in the IN position, the time duration and relative delay position of the normal resolution aper-

* -200 V not provided at rear-panel connector in early units.

ture time may be remotely controlled at this input. The required input is a zero-based (±1 V) pulse which reaches at least +3 V. The input impedance is 5 kΩ (min.) Input voltages greater than ±12 V are clamped to those power supply levels and may cause internal damage if exceeded. This input is disconnected if the associated switch is set to OUT. This input is active only if operating in the normal resolution mode. The minimum achievable aperture time is 0.5 μs.

To use the Model 160 in the "external gate mode", the following procedure is suggested.

(1) Set the Trigger Mode switch to EXT.

(2) Disconnect any input trigger signal from the Trigger IN BNC jack.

(3) Set the rear-panel External Gate toggle switch to IN.

(4) Apply the external gate signal.

SCAN/DELAY

(1) OUTPUT

Provides a 0-to-10 V (maximum range) positive voltage for the abscissa drive of an X-Y plotter or storage oscilloscope. The 10 V full-scale output corresponds to 100% of time base. This output ramps over a voltage range determined by the setting of the Initial and Final Delay dials. For example, if the Initial Delay dial were set to 20% and the Final Delay dial were set to 80%, the output would ramp from +2 V to +8 V. If the front-panel Scan Mode switch is in the DELAY position, the output is a fixed dc voltage (range 0-to-10 V) proportional to the setting of the Initial Delay dial. If the Scan Mode switch is transferred to HOLD during a scan, the output voltage will hold at the level reached at the moment of transfer.

(2) INPUT

When the Scan Rate switch is set to EXT, a dc level applied to this connector will position the aperture along the time base, with the delay proportional to the applied voltage. The applied voltage must be in the range of 0 V to +10 V and the scale factor is 1 V per 10% of time base. The input resistance is nominally 5000 ohms, with clipping at ±12 V. Input levels greater than ±50 V can damage the input circuitry. The rate of change of the input signal should not exceed 10 V/ms (and normally will be very much slower) for accurate tracking between the input voltage and the delay. Possible applications include the following.

(a) Scan function controlled by an external experimental parameter such as magnetic field, light intensity, etc.

(b) Scan function is deliberately made non-linear to optimize the experimental time.

(c) The scan function is made to reverse for the purpose of examining "hysteresis" phenomena.

To operate the Model 160 in this mode, one might proceed as follows.

(a) Set the Scan Rate switch to EXT.

(b) Set the time base, aperture time, etc., as per normal operation.

(c) Set the Final Delay dial to 100%. Other delay settings will cause the Tilt light to turn on if the external delay input function "crosses over" the final delay setting.

(d) Apply the external scan voltage from a low impedance source (less than 100 ohms).

TIME BASE INPUT/OUTPUT

(1) OUTPUT

The output signal at this connector is a replica of either the internal or external time base function. The output voltage is nominally a 0-to-10 V positive ramp capable of delivering up to 2 mA to an external load. This output, besides being useful for troubleshooting, serves as a time base reference to external equipment.

(2) INPUT

This input, when activated by setting the front-panel Time Base Mode switch to EXT, allows use of an externally derived time base. A 0-to-10 V (positive) signal corresponds to a 0-to-100% delay (±2%). The input resistance is nominally 100 kilohms, but the input voltage should not exceed -10 V or +50 V. When operating in this mode, all timing, synchronization, and holdoff considerations are controlled externally. The maximum external input time base repetition rate should not exceed 100 kHz, with a maximum ramping-rate limit of +10 V/μs. In any case, to be assured that all processes are completed, the repetition period should be no shorter than the sum of:

TB] ext. + AT + ST + MT,

where TB] ext. = duration of external time base ramp including flyback time

AT = Aperture Time
ST = Stretch Time (10, 30, or 100 μs)
MT = Memory storage time for analog storage accessory, if used. Typically 5 ms.

A "non-obvious" application of the External Time Base Input is to allow external control of the aperture position during high resolution mode operation. (The External Gate Input is useful in the normal

resolution mode only.) To externally control the position of the aperture, one might proceed as follows.

(a) Set the Time Base Mode switch to EXT. and supply a rectangular pulse to the External Time Base Input. The internal aperture strobe pulse will be generated when the leading edge of the applied pulse "crosses over" the threshold set by the internally or externally generated "delay" voltage. By positioning the input pulse relative to the trigger time of the experiment, the aperture strobe is positioned as well. The minimum threshold is about 0.2 V with a typical hysteresis of about 5 mV rms.

(b) Set the aperture time in the usual manner, that is, by means of the front-panel controls.

PRE-AMP OUTPUT

An inverted (180° phase difference) replica of the preamplifier output appears at this connector (output impedance approximately 300 ohms)*. With a full scale input signal, the output is approximately 0.5 V into a high impedance load or approximately 70 mV when terminated with 50 Ω. When observing high-frequency phenomena, one should use a fifty ohm cable which is terminated in fifty ohms at the receiving end of the line. The bandwidth at this output has an upper frequency limit of about 10 MHz.

3.6 PITFALLS

In an instrument as complex as the Model 160, it is almost inescapable that there will be a few "non-obvious" factors which can confuse an operator. Frequently, the search through the instruction manual to find the few lines relating to the "problem" can be a considerable task. As a convenience to the operator in avoiding such a search, several of the "pitfalls" relating to operation of the Model 160 are gathered together here into a single subsection as follows.

(1) Front Panel Gate Output

The buffer circuit between the internal gate drive circuits and this output is not as "fast" as the gate drive circuits themselves. Normally, this is not noticeable. However, when operating with very short aperture times in the high resolution mode, a pronounced delay and stretching of the gate pulse becomes apparent. The delay is approximately 30 ns and the stretch is typically in the range of 30 ns to 50 ns. Although this may be disconcerting when monitoring the gate output with an oscilloscope, it does not in any way signify that the signal is not being sampled at the proper time and for the proper duration.

(2) Delay Between Triggering and Time Base Generation

Between application of a trigger and initiation of a time base ramp,

* In early units full scale output is approximately 1 V from 600 Ω.

MODEL 160 FRONT-PANEL CONTROLS AND CONNECTORS

LABEL	TYPE	FUNCTION
TRIGGER MODE		
EXT.	3 pos. switch Switch pos.	Determines mode of triggering. Instrument triggered from external source.
RECURRENT	Switch pos.	Instrument "free runs".
CONT. GATE	Switch pos.	No triggering. Gate conducts continuously.
DELAYED TRIGGER MODE	2 pos. toggle	Determines whether Delayed Trigger output will be scanned or adjustable.
DIAL	Switch pos.	Trigger Delay given by setting of Output Trigger Delay dial.
SCAN	Switch pos.	Trigger Delay controlled by scan circuits.
OUTPUT TRIGGER DELAY	10 turn dial	Controls the position of an internally-derived, delayed trigger output. Delay position calibrated as a percentage of time base.
TRIGGER SLOPE	2 pos. switch	For external triggering. Determines whether the Model 160 will be triggered on the positive (+) or negative (-) slope of the trigger waveform.
TRIGGER THRESHOLD	Potentiometer	For external triggering. Determines trigger point based on amplitude. Range is -5 V through +5 V.
TRIGGER INPUT	BNC jack	External trigger applied. Minimum amplitude 0.3 V.
DELAYED TRIGGER OUTPUT	BNC jack	Delayed trigger output reference. Amplitude 1 V.
TIME BASE		Switch setting determines 100% delay range.
INT.	22 pos.switch	
EXT.	Switch pos.	22 position switch ineffective. 100% delay range determined by externally derived 0 to +10 V ramp.
SCAN/DELAY		
INITIAL DELAY	10 turn dial	Determines delay between trigger and aperture opening. Calibrated as percentage of time base.
FINAL DELAY	10 turn dial	Determines maximum delay in a given time base range. Calibrated as percentage of time base.
DELAY MODE		
DELAY	Switch pos.	Delay is set by Initial Delay dial.
SCAN	Switch pos.	Aperture Delay is automatically increased over the range determined by the setting of the Initial and Final Delay dials.
HOLD	Switch pos.	Allows delay, when scanning, to be "stopped" at any point over the scanned delay range.
SCAN RATE	10 pos. switch	Determines the full-scale rate at which the aperture gate is scanned through the time base range.
EXT.	Switch pos.	All delay functions controlled by externally derived 0 to 10 V dc voltage.
SCAN RESET	Pushbutton	Scan delay automatically resets to that delay set by the Initial Delay dial.
REPEAT SCAN	Switch pos.	Scan automatically repeats.
SINGLE SCAN	Switch pos.	Single scan only.
APERTURE TIME	Dual-concen. control	Controls duration of sampling gates from 10 ns to 0.55 s. Aperture time = Range x Multiplier.
BLUE RANGE	3 pos.	Automatically enables high-resolution mode.
RED RANGE	6 pos.	Automatically enables normal mode.
TIME CONSTANT (ns to µs A.T.)	12 pos.switch (blue)	Primary time constant control when operating in high resolution mode.

MODEL 160 FRONT-PANEL CONTROLS AND CONNECTORS (Cont.)

LABEL	TYPE	FUNCTION
TIME CONSTANT (µs to ms A.T.)	14 pos.switch (red)	Time constant control in normal resolution mode.
STRETCH TIME	3 pos.toggle	Determines stretch time of integrator when operating in high resolution mode. Improves high resolution mode duty factor limit. Normal setting is 30 µSEC.
RETENTION	Potentiometer w/OFF switch	Improves transfer and averaging accuracy in high resolution mode.
PREFILTER	9 pos.switch	Introduces low-pass filter before amplifiers to reduce noise.
INPUT COUPLING	3 pos.switch	Determines whether input coupling will be AC, DC, or GRD.
INPUT SENSITIVITY	9 pos.switch	Determines sensitivity and allows gain calibration.
VOLTAGE	8 positions	Sets full-scale input sensitivity.
CAL.	1 position	Provides full-scale calibrate signal.
INPUT SWITCH	2 pos.switch	Selects input impedance.
50 Ω	Switch pos.	Input impedance 50 Ω.
100 kΩ	Switch pos.	Input impedance 100 kΩ.
100 kΩ INPUT	BNC jack	Provides signal input impedance of 100 kΩ.
50 Ω INPUT	BNC jack	Provides signal input impedance of 50 Ω.
RESET (MEMORY)	Pushbutton	Resets and disables analog memory.
MEMORY	On-off toggle	Actuates analog storage circuits (if installed).
ZERO	Potentiometer	Provides ± full-scale internal offset.
INPUT OFFSET	10 turn dial	Provides calibrated offset at input.
OFFSET SCALE	Toggle switch	Changes input offset range from 100% to 1000% F.S.
OFFSET POLARITY	Toggle switch	Determines whether input offset will be positive, negative, or off.
GATE OUT	BNC jack	Provides reference marker pulse coincident with the sampling pulse. Pulse width is equal to aperture time except when "1 nSEC." aperture time range is selected.
OUTPUT	BNC jack	Provides ±10 V out for ± full-scale in.

INDICATOR LIGHTS

LIGHT NAME OR IDENTIFICATION	INDICATION
METER ILLUMINATION	Power on
OVERLOAD	Input signal too large, approximately ten times full-scale in the normal resolution mode and approximately 3.5 times full scale in the high resolution mode.
TILT (fully on)	Initial Delay exceeds Final Delay or Single scan is completed.
TILT (flashing)	Aperture time exceeds time base duration or Aperture time overlaps time base range or Unit is operating in External Time Base mode.
MEMORY	Indicates that analog storage memory mode is enabled (if installed).

MODEL 160 REAR-PANEL CONNECTORS AND CONTROLS

LABEL	TYPE	FUNCTION
PRE-AMP OUTPUT	BNC jack	Inverted output of internal amplifier. Gain approximately 25 through 300 ohm source impedance. Bandwidth approximately 10 MHz into 50 ohm termination.
TIME BASE		
EXT. INPUT	BNC jack	External time base ramps (0 to +10 V) may be used to determine time base range. Z_{in} = 100 kΩ.
OUTPUT	BNC jack	Buffered output of time base ramp (internal or external). Z_{out} = 100 Ω.
SCAN/DELAY		
EXT. INPUT	BNC jack	External dc voltage from 0 V to +10 V controls aperture delay over the time base range.
OUTPUT	BNC jack	Zero to +10 V dc output signal proportional to the aperture delay. May be used for abscissa drive of an X-Y recorder.
EXT. GATE		
INPUT	BNC jack	Zero to +5 V minimum pulse will control the timing and width of the aperture when in the normal resolution mode.
IN/OUT	Switch	IN position enables Ext. Gate Pulse function. Front-panel Trigger Mode switch should be set to EXT. TRIGGER. OUT position disables Ext. Gate Pulse function.
OUTPUTS		Output signals for ± full-scale input.
NORMAL	BNC jack	±10 V at 1000 Ω.
INVERTED	BNC jack	±10 V at 1000 Ω (inverted).
RECORDER	BNC jack	±1 mA to drive galvanometric recorders.
RECORDER ADJUST	Potentiometer	Adjusts recorder output current ±50%.
INTERFACE	14 pin con.	Key signals and power voltages available. See separate list.
LINE VOLTAGE	2 pos.switch	Allows operation from either 115 Vac or 230 Vac.

INTERFACE CONNECTIONS

PIN	DESCRIPTION
A	0 V (signal and power ground)
B	+24 V
C	-24 V
D	+4.5 V
E	+12 V
F	-12 V
J	-200 V*.
H	+ DC OUTPUT (parallel with Normal Output BNC jack)
K	SCAN/DELAY Output
P	EXT. CAPACITOR (outside foil connection)
R	EXT. CAPACITOR (integrator summing junction)

* -200 V not provided in early units.

Table III-6. CONTROLS, CONNECTORS, AND INDICATORS

there is an irreducible delay of about 150 ns. As a result, one cannot recover signal information in the first 150 ns after triggering, unless one uses the delayed trigger feature to trigger the experiment as discussed under DELAYED TRIGGER OUTPUT on page III-7. Alternatively, one might consider routing the input signal through 150 feet of cable.

(3) Minimum Setting of Initial Delay Dial

If the Initial Delay Dial is set to less than 5%, it may happen that, even though normal time base triggering is taking place, gate pulses are not produced. Without gate pulses, the gate never opens and the result is the same as if the instrument were not being triggered at all. This is a normal condition, and in no way indicates malfunctioning. A convenient way to check gate pulse generation when operating with Initial Delay Dial settings of less than 5% is to monitor the Gate Output jack with an oscilloscope. If it is necessary to examine signals in the first few percent of the time base range and gate pulses are not being generated properly, one can simply select a shorter time base range, in which case a higher delay dial setting will be required to position the aperture opening on the corresponding signal point.

Similarly, when scanning, no gate pulses may be produced for an interval corresponding to the scanning of the first few percent of time base. Note that, with a long scan period (maximum 1000 minutes), this "dead time" can be fairly lengthy.

(4) Rear-Panel Preamplifier Output

The output of the wide-band preamplifier is provided at the rear panel of the instrument. The bandwidth of this output is approximately 10 MHz, considerably less than the overall instrument response. Also, the frequency response at this output reflects "tailoring" of the preamplifier for the best overall instrument frequency response, and so is not directly indicative of the overall instrument response. In other words, one should not evaluate the frequency response of the Model 160 by applying an input square wave and monitoring the signal at the rear-panel Preamplifier output.

(5) Retention Control

Take careful note that the Retention control is rotated clockwise to increase the retention, and counterclockwise to decrease it. When the Retention control is fully counterclockwise, the retention is off. In other words, the Retention control functions exactly as indicated by the "arrows" in the Retention control panel symbolization. Because of the position of MAX and OFF in the symbolization, an operator proceeding quickly might mistakenly assume the control works "backwards".

IMPORTANT BOXCAR INTEGRATOR RELATIONSHIPS

1. OBSERVED TIME CONSTANT (OTC)

   (a) Normal Resolution Mode

   $$OTC = \frac{TC]_{NR}}{(AT)\,f} \text{ seconds}$$

   (b) High Resolution Mode

   $$OTC \simeq \frac{1}{f}\sqrt{\left(\frac{TC]_{HR}}{AT}\right)^2 + \left(\frac{TC]_{NR}}{ST}\right)^2} \text{ seconds}$$

   or, for $\frac{TC]_{NR}}{ST} << \frac{TC]_{HR}}{AT}$, $OTC \simeq \frac{1}{f}\,\frac{TC]_{HR}}{AT}$ seconds

   or, for $\frac{TC]_{NR}}{ST} >> \frac{TC]_{HR}}{AT}$, $OTC \simeq \frac{1}{f}\,\frac{TC]_{NR}}{ST}$ seconds

2. SIGNAL-TO-NOISE IMPROVEMENT RATIO (SNIR)

   $$SNIR = \sqrt{\frac{2TC}{AT}} \text{ or } \sqrt{2(OTC)f}\,,^{*} \text{ providing a period of five times the OTC has elapsed.}$$

3. TIME CONSTANT (TC)

   (a) In Normal Resolution Mode, Time Constant is that selected by red-symbolized Time Constant switch.

   (b) In High Resolution Mode, Time Constant is obtained by multiplying OTC (computed by one of the formulas in "1" above) by (AT)f.

   Note that, if $\frac{TC]_{NR}}{ST} << \frac{TC]_{HR}}{AT}$, $TC \simeq TC]_{HR}$.

4. MINIMUM SCAN RATE (MSR)

   $$MSR = \frac{TC \times TB}{12 \times f \times (AT)^2} \text{ minutes, or. } MSR = \frac{TB \times OTC}{AT \times 12}{}^{*} \text{ minutes.}$$

ABBREVIATIONS USED IN THE ABOVE FORMULAS

- TC = Time Constant
- $TC]_{HR}$ = Setting of blue-symbolized Time Constant switch.
- $TC]_{NR}$ = Setting of red-symbolized Time Constant switch.
- ST = Stretch Time
- AT = Aperture Time
- f = Repetition frequency

* Formulas based on OTC frequently prove more convenient for High Resolution Mode computations, though they are equally valid for Normal Resolution Mode computations.

Table III-7. IMPORTANT BOXCAR INTEGRATOR RELATIONSHIPS

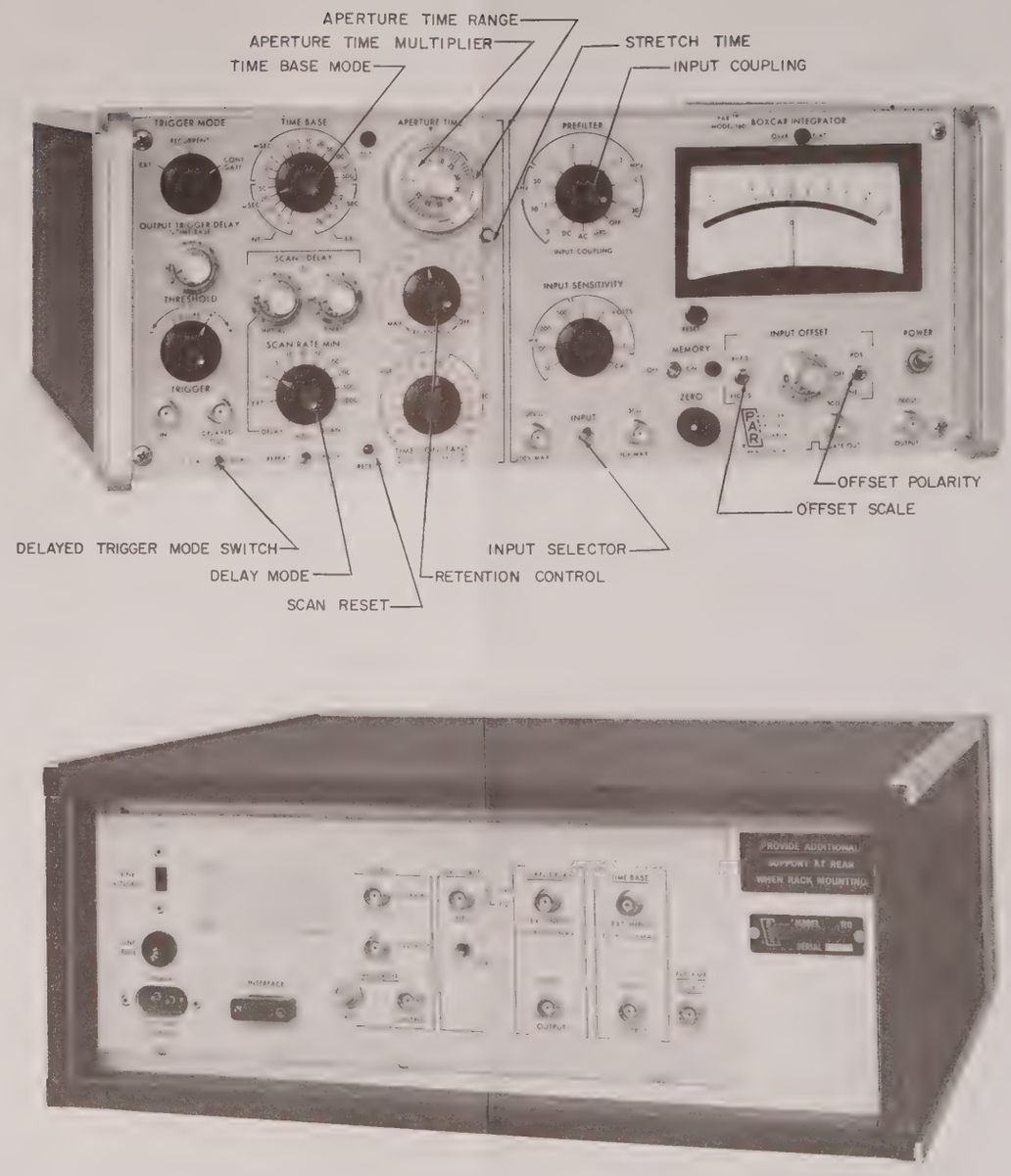


Figure III-13. MODEL 160 BOXCAR INTEGRATOR (front and rear views)

SECTION IV
THEORY AND CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The purpose of this section of the manual is to discuss the functioning of the Model 160 Boxcar Integrator on both the block diagram and circuit analysis levels. This material is provided for two reasons. First, a researcher interested in the detailed workings of the instrument will be able to satisfy his curiosity. Second, should it ever be necessary to troubleshoot the instrument, this section should prove a source of valuable information.

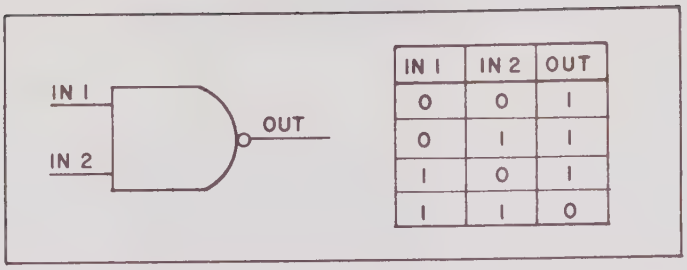
The Model 160 Boxcar Integrator can be considered to comprise two principal subsystems, namely a Signal Channel Subsystem and a Timing Channel Subsystem. The former processes the applied signal and provides the gated and averaged output. The latter determines when and for how long the instrument averages with each repetition of the input signal. For a simple generalized discussion of how the signal processing and timing is done, refer to subsection 3.3 (page III-2). Subsection 3.3 provides good background material for the following detailed discussions, which are divided into three major sections. First the Timing Channel is discussed on a block-diagram level. Then the Signal Channel is discussed on a block-diagram level. Last, the circuits themselves are covered in detail with many references to the schematics, which are found at the end of the manual. These schematics "fold out" for easy access.

However, before going directly into the timing channel discussion, two additional topics will be briefly reviewed, namely NAND Gate Logic and Tunnel Diodes. This is done because the Model 160 uses NAND gate logic extensively to control timing functions and because several circuits employ tunnel diodes to achieve fast switching times. The brief reviews which follow should make it easier to understand the detailed discussions.

4.2 NAND LOGIC

The Model 160 uses positive NAND logic, that is, a digital "1" is a positive voltage (nominally +4.5 V, +2 V min.) and a digital "0" is approximately zero volts or ground. When a logic line is at the "1" level, it is referred to as being "up". When it is at the logic "0" level, it is referred to as being down. A NAND gate can be regarded as an AND gate with its output inverted. In the case of an AND gate, all the inputs must be up for the output to be up. If any one of the inputs is down, the output will be down. For a NAND gate the situation is reversed, that is, all of the inputs must be up for the output to be down. If any one of the inputs is not up, the output will not be up. This behavior is illustrated by the following "truth table", which is accompanied by the schematic representation of a typical NAND gate with labels to identify the inputs and output.

Note that a single change of state of one of the input lines does not necessarily change the output state. For example, if both inputs were initially down, the output would be as shown. If one of the inputs were to then switch to the up state, the output would still remain up; both inputs must be up for



IN 1	IN 2	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Figure IV-1. SYMBOL AND TRUTH TABLE FOR NAND GATE

the output to go down. The illustrated gate has two inputs. However, it could as easily have many more inputs or but a single input. The circuit would still behave in the same manner, that is, all inputs would have to be up for the output to be down. It might be mentioned that two or more inputs can be paralleled together, if desired, in which case they function as a single input. In the Model 160, most of the gates have two inputs but a few have three.

Functions monitored and controlled by the gates in the Model 160 include trigger slope detection, time base inhibiting, and tilt indications. The block diagram discussions which pertain to these functions must necessarily refer to the controlling logic in some detail. A separate truth table is provided for each gate or group of gates according to the function(s) being considered. In Figure IV-4, a block diagram of the Timing and Logic circuits, these gates are identified by "G" numbers for easy referral. These G numbers do not appear on the schematics, where the individual gates are simply identified according to the integrated circuit of which they are a part. All those common to integrated circuit A1 (or A2, or A3, etc.) are so identified, with numbers provided on the input and output lines to indicate the gate function associated with any given pin of the integrated circuit. Each schematic is accompanied by a parts location diagram which shows the location of all the components on the corresponding circuit board.

4.3 TUNNEL DIODES

Tunnel diodes differ from ordinary diodes in that they exhibit the negative resistance characteristic illustrated in Figure IV-2. As a tunnel diode is forward biased, the current through it increases almost linearly with increasing bias until the voltage reaches Vp (peak voltage). Beyond this point the current decreases with increasing forward bias until the bias voltage reaches Vv (valley voltage), the minimum current point. From here the current increases steeply with increasing forward bias, following the characteristic curve of other diodes. The ratio of the current at Vp to that at Vv, referred to as the peak-to-valley ratio, is generally in the range of 10:1 to 15:1. This negative resistance characteristic of the tunnel diode allows it to be used as an amplifier, as an oscillator, and as a rapid switching device, its use in the Model 160.

To see how the tunnel diode is used to speed switching times in the Model 160

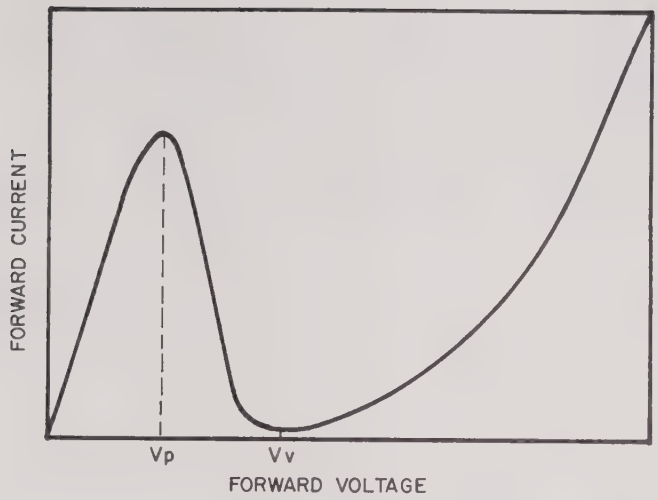


Figure IV-2. TUNNEL DIODE CHARACTERISTIC CURVE

timing circuits, consider the circuit shown in Figure IV-3. Quiescently transistor Q1 is cut off and resistor R1 supplies a small bias current to tunnel diode CR1 and resistor R2. The resistance of R1 has been selected such that the diode is at point A of its characteristic curve, a point just below the peak in the first positive region. Most of the current supplied by R1 flows through the diode, which has a resistance smaller than that of R2 in this region. The voltage drop across the diode is small because of its low resistance. Assume now that the input pulse is applied. As Q1 begins to conduct, the current through CR1 increases to the peak and then crosses over

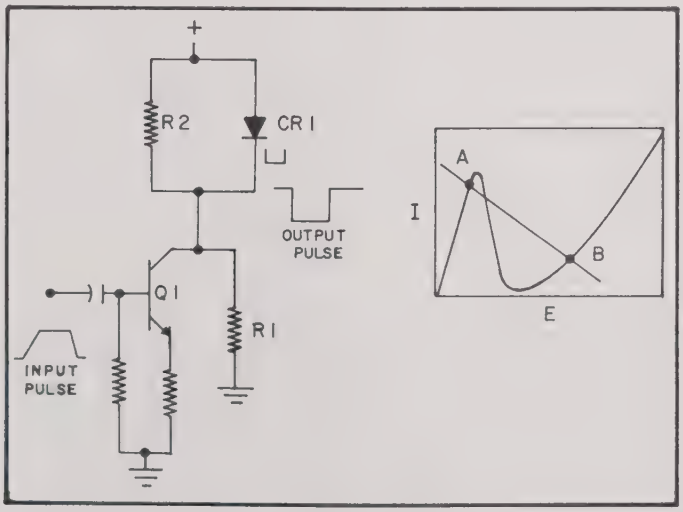


Figure IV-3. TUNNEL DIODE SWITCHING CIRCUIT

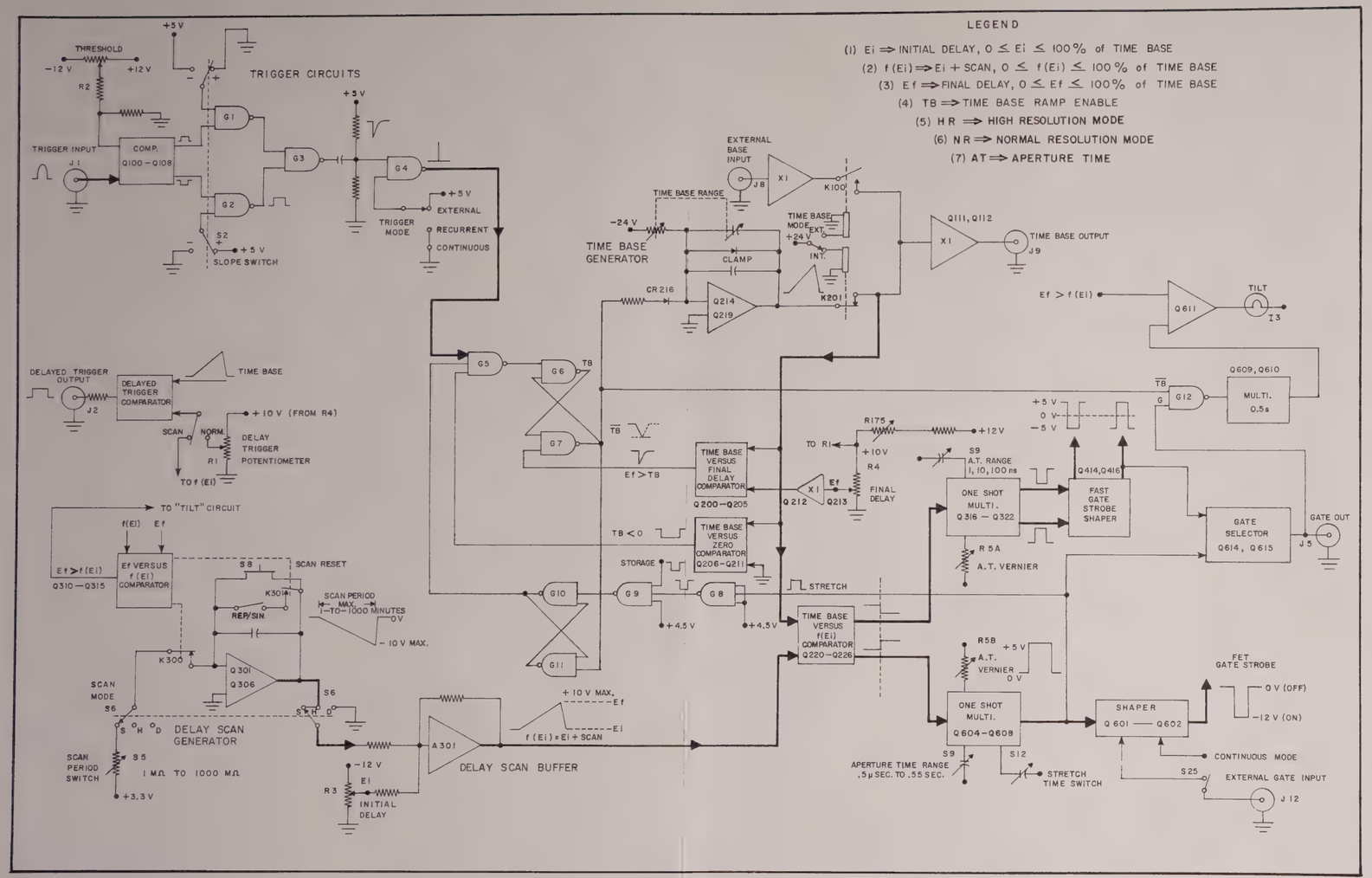


Figure IV-4. BLOCK DIAGRAM OF TIMING AND LOGIC CIRCUITS

into the negative resistance region. The resistance of the diode increases greatly and its operating point must shift to a different spot on the curve according to the current available and the drop across the R2-CR1 parallel circuit. Point B, the new operating point in the second positive resistance region, is determined by the value of R2 and the magnitude of the current supplied by Q1 (assuming this current is large relative to that supplied by R1). The transition from A to B is extremely fast, and a correspondingly fast increase in the voltage drop across the diode occurs. This voltage drop constitutes the leading edge of the output pulse and is very much faster than the rise time of the input pulse which caused the diode to switch.

The diode remains at point B for the duration of the input pulse. When the pulse ends, the diode switches back to point A. However, because the "hump" from point B to the negative resistance region is not as "steep" as the hump from point A to the negative resistance region, the fall time of the output pulse is not as fast as the rise time.

Nevertheless, both the leading and trailing edges are significantly sharpened by using the tunnel diode switching circuit.

4.4 TIMING AND LOGIC

TRIGGER CIRCUITS

Referring to Figure IV-4, a block diagram of the Time and Logic circuits, notice that input triggers are applied to J1, the Trigger Input jack. From here, the positive trigger pulse (it could as easily have been negative) is routed to the Trigger Comparator circuit where it is detected with respect to the threshold voltage as determined by the setting of the Threshold control. As the leading edge of the Trigger pulse crosses over the threshold voltage, the complementary comparator output changes state. It reverts to its original state when the trailing edge of the Trigger pulse crosses over the threshold voltage in returning to its quiescent level.

As shown in Figure IV-4, the comparator output is applied to NAND gates G1 and G2, which do the slope detection. These gates in turn drive another gate G3. Its output in turn is capacitively coupled to a fourth gate G4, which provides a trigger to the Time Base Generator control circuits if the instrument is operating in the External Trigger mode. Table IV-1 shows the truth table applicable to gates G1 through G4 when the instrument is triggered from the positive slope of a positive trigger pulse. Because of the differentiation provided by the RC coupling network, G4 always yields a transient output pulse, even for relatively long input triggers.

	G1			G2			G3			G4			ACTION
CONDITION	IN1	IN2	OUT	IN1	IN2	OUT	IN1	IN2	OUT	IN1	IN2	OUT	
QUIESCENT	0	0	1	1	1	0	1	0	1	1	1	0	
POSITIVE TRIGGER BEGINS	0	1	1	0	1	1	1	1	0	0→1	1	1→0	+ TRIGGER TO G5
POSITIVE TRIGGER ENDS	0	0	1	1	1	0	1	0	1	1	1	0	QUIESCENT RESTORED

Table IV-1. TRIGGER LOGIC TRUTH TABLE

Other truth tables could be constructed to show that the output pulse from G4 can be made coincident with either the leading or trailing edge of either positive or negative input triggers, according to the position of the Slope switch. Notice that G4 provides a transient output trigger in the External Trigger mode only. In the Recurrent and Continuous modes, input 2 of G4 is locked down and the output of the gate is continuously up regardless of whether or not triggers are applied to J1. The consequence of this action is to allow the Time Base Generator to run regeneratively as explained in the following paragraphs.

TIME BASE GENERATOR AND CONTROL CIRCUITS

Referring to Figure IV-4, note that the Time Base Generator is an operational amplifier connected as an integrator. There are two inputs to the summing junction, one a resistive current source fed from -24 V and the other diode CR216, which is driven by the control logic. When the control logic output is up, and CR216 therefore forward biased, the Time Base Generator is controlled by the control logic because the impedance of this line is much lower than that of the current source. When the logic output is down, and CR216 therefore reverse biased, the Time Base Generator is controlled by the current source because of the extremely high reverse bias resistance of CR216.

In the quiescent state, the output of the control logic is up and CR216 is forward biased. In response to this low impedance positive input, the output of the amplifier is negative. However, the clamping diode around the amplifier prevents the amplifier output from going more than a fraction of a volt negative.

When a trigger is applied, the control logic output goes down, reverse biasing CR216 and transferring control of the Time Base Generator to the current source. The generator output immediately begins to ramp positively at the rate of i/C volts per second, where "i" is the current supplied by the current source and C is the capacitance around the generator. Both the current and capacitance are a function of the setting of the Time Base switch. This ramping continues until the ramp voltage crosses over the voltage (full scale +10 V) picked off the Final Delay potentiometer, at which time the control logic output is switched positive. The generator output then begins ramping negatively. However, because the impedance of the logic control line is much lower than that of the current source, the negative ramping is correspondingly faster to achieve a fast reset. This negative ramping continues until the clamping diode becomes forward biased to restore the quiescent state.

The output of the Time Base Generator is routed to a buffer amplifier and to four comparator circuits. Two of these function as part of the time base and trigger control logic. The third triggers the gate monostables, and the fourth provides the Delayed Trigger Output. Note that provision is made for using an externally derived time base function when the Time Base Mode switch is set to EXT.

The control logic can functionally be divided into two portions. Gates G5, G6, and G7, together with the Time Base versus Final Delay Comparator, control the Time Base Generator. Gates G8, G9, G10, and G11, together with the Time Base versus Zero Comparator, provide trigger inhibit functions. This

CONDITION	G5				G6			G7			ACTION
	IN1	IN2	IN3	OUT	IN1	IN2	OUT	IN1	IN2	OUT	
QUIESCENT	0	1	1	1	1	1	0	0	1	1	
TRIGGER FROM G4	1 → 0	1	1	0 → 1	0 → 1	0	1	1	1	0	CR216 REVERSE BIASED, RAMP BEGINS
RAMP IN PROGRESS	0	1	0	1	1	0	1	1	1	0	IN 3 of G5 INHIBITS FURTHER TRIGGERING
RAMP EXCEEDS Ef	0	1	0	1	1	1	0	0	0	1	G6/G7 SWITCH, RAMP RESETS
RAMP CROSSES ZERO	0	1	1	1	1	1	0	0	0	1	QUIESCENT CONDITIONS RESTORED

Table IV-2. TRUTH TABLE FOR TIME BASE CONTROL LOGIC

division into two groups, though admittedly somewhat "artificial" in that the two groups do work together, does nevertheless simplify understanding the operation of the circuits.

First consider the Time Base Control logic, using as references Figure IV-4 and Table IV-2, a truth table of the Time Base Control logic when operating in the External Trigger mode.

Gate G5, providing its inhibit inputs, inputs 2 and 3, are up, passes any trigger pulse from G4 to the "latch pair", G6 and G7. In the quiescent state, the output of G6 is down and the output of G7 up, forward biasing CR216 and holding the ramp generator in the reset state.

Assume a trigger is applied. The latch pair switches as indicated in Table IV-2, reverse biasing CR216 and allowing a ramp to begin. As soon as the rising ramp voltage crosses zero, the output of the Time Base versus Zero Comparator goes down, applying a "0" to input 2 of G5, and thereby inhibiting G5 from passing any more trigger pulses for as long as the comparator is in this state, that is, for the duration of the time base ramp. When the ramp crosses over the final delay voltage, as determined by the setting of the front panel Final Delay dial, the Time Base versus Final Delay Comparator provides a negative input to G7, switching the latch pair back to their initial state. Diode CR216 is again forward biased and the ramp resets. Note that the negative output of the Time Base versus Final Delay Comparator is transitory; as soon as the reset begins, the comparator reverts to its quiescent state. As the resetting ramp crosses zero, the Time Base versus Zero Comparator also switches, removing the inhibit from input 3 of G5. The entire Time Base Control logic is now restored to its quiescent state and may be triggered again.

In the Recurrent and Continuous gate modes, the operation differs because the output of G4 is locked up, whether or not triggers are applied. As a result, G5 "sees" a continuous trigger command, and, as soon as one ramp ends, another begins. Of course, the inhibit limitations imposed at inputs 2 and 3 of G5 still apply.

Gates G8 through G11 provide the stretch and storage functions by providing an appropriately timed "0" to input 2 of G5. The stretch inhibit function is effective each time the normal resolution monostable "fires". Thus, "stretch" inhibiting is provided not only during the stretch time for high

resolution operation, but also during the normal gate-open time for normal resolution operation. The output of the Q604-Q608 monostable is applied to G8 to achieve the "stretch" inhibit function. Gate G9 prevents triggering during the 5 ms analog storage period. Storage inhibiting, of course, applies only to instruments equipped with this option. Gates G10 and G11 constitute another latch pair, with G10 providing the actual inhibit output to G5.

Note that if the stretch/storage periods are fully within the time base ramp duration, the corresponding inhibiting is redundant to that already provided by the time base ramp in progress inhibiting at pin 3 of G5. However, it can easily occur that the stretch or storage time will extend well beyond the ramp interval itself, in which case the stretch/storage inhibiting action is essential to prevent a new ramp from being triggered before the stretch/storage circuits have recovered. Table IV-3 is a truth table showing a complete cycle of the trigger inhibiting logic. Note that the underlying assumption in preparing the table was that the stretch time ends first, then the storage time, and last the ramp. Similar tables could be prepared for the various possible time combinations of stretch, storage, and time base.

	G8			G9				G10			G11			
CONDITION	IN1&3	IN2	OUT	IN1	IN2	IN3	OUT	IN1	IN2	OUT	IN1	IN2	OUT	ACTION
QUIESCENT	1	0	1	1	1	1	0	0	0	1	1	1	0	
RAMP IN PROGRESS	1	0	1	1	1	1	0	0	1	1	1	0	1	G11 SWITCHES
STRETCH AND STORAGE BEGIN	1	1	0	0	0	1	1	1	1	0	0	0	1	G10 SWITCHES, INHIBITING BEGINS
STRETCH ENDS	1	0	1	0	1	1	1	1	1	0	0	0	1	G8 SWITCHES
STORAGE ENDS	1	0	1	1	1	1	0	0	1	1	1	0	1	G10 SWITCHES, INHIBITING ENDS
RAMP EXCEEDS Ef	1	0	1	1	1	1	0	0	0	1	1	1	0	QUIESCENT CONDITIONS RESTORED

Table IV-3. TRUTH TABLE FOR TRIGGERING INHIBITING LOGIC

TIME BASE VERSUS f(Ei) COMPARATOR

This comparator supplies trigger commands to the two gate pulse monostables when the time base crosses over f(Ei), a voltage equal to the sum of the scan generator output and the voltage picked off the Initial Delay potentiometer. In this manner, the gate, either Q600 in the normal resolution mode, or both Q600 (as a stretcher) and the fast sampling bridge in the high resolution mode, is made to open at the proper time.

Referring to Figure IV-4, note that f(Ei) is the sum of the scan generator output and the voltage picked off the Initial Delay dial. These two levels are summed by the Delay Scan Buffer Amplifier when the Delay Mode switch is set to SCAN or HOLD. When this switch is set to DELAY, the scan generator output is disconnected from the buffer and f(Ei) is simply Ei, the initial delay voltage. The Initial Delay dial is calibrated in percent of time base, allowing precise positioning of the aperture opening on the time base interval. For example, if the dial were set to 20%, and the time base to 10 ms, 2 ms after triggering the time base ramp will cross f(Ei) and the Time Base versus f(Ei) Comparator will provide trigger outputs to the monostables.

If the Delay Mode switch is set to SCAN, the Scan Generator will be ramping and this ramp voltage will be summed with the Initial Delay voltage. As a result, f(Ei) will increase linearly at the scan rate and successive time base ramps will cross over f(Ei) later in time relative to the trigger time. Consequently, the aperture is positioned a little later with each successive time base. In effect, the aperture is swept over the time base interval at the scan rate.

When the scan ramp is zero, f(Ei) has its minimum value, and is equal to the initial delay. Thus the minimum delay between triggering and aperture opening is the dialed initial delay. As the scan ramp advances, the delay increases. The maximum delay is determined by the setting of the Final Delay dial, which, as explained in the earlier discussion of the Time Base Generator, governs the termination of the time base ramp. Thus the aperture position is scanned over that portion of the selected time base period determined by the setting of the Initial Delay and Final Delay dials, with the scan rate determined by the setting of the Scan Period switch.

If the Delay Mode switch is set to HOLD, the scan ramp holds at the level reached when the switch was transferred to that position. f(Ei) holds as well and with each successive time base ramp, the aperture opens at the same time. Scanning resumes from the "hold" point if the Delay Mode switch is returned to the SCAN position.

DELAY SCAN GENERATOR

Like the Time Base Generator, the Delay Scan Generator is an operational amplifier connected as an integrator type ramp generator. Unlike the Time Base Generator, the Scan Ramp Generator produces very slow ramps, ranging from one minute to 1000 minutes for a full scan according to the position of the Scan Rate switch.

Referring to Figure IV-4, note the many switches and relays associated with the Delay Scan Generator. The Scan Period switch determines the magnitude of the ramping current and hence the ramping rate. Resistors ranging from one megohm to 1000 megohms are connected between +3.3 V and the summing point according to the switch position. Note that the integrating capacitance remains constant for all ramping rates, this in contrast to the Time Base Generator where both the resistance and the capacitance vary as a function of the selected time base range.

The Scan Mode switch acts at both the input and output of the Delay Scan Generator. At the input, it is interposed between the current source and the summing junction. In the SCAN position, current is supplied from the positive 3.3 volt source and the generator output can ramp negatively. In the other two positions, HOLD and DELAY, current is withheld and no ramping can occur. At the output, contacts of this switch supply the Scan Generator output to the Delay Scan Buffer when the Delay Mode switch is set to SCAN or HOLD as explained in the preceding discussion of the Time Base versus f(Ei) Comparator. In the DELAY position, that input to the Delay Scan Buffer is grounded and the buffer "sees" the Initial Delay potentiometer only.

Last, the Scan Reset Pushbutton allows the operator to reset the ramp to zero

at any time by discharging the integrating capacitor.

Ef VERSUS f(Ei) COMPARATOR

This circuit operates in conjunction with the Delay Scan Generator to terminate a scan if f(Ei) exceeds Ef. It also provides an output to the Tilt circuit to warn the operator of this condition. The comparator controls the scan duration by actuating two relays, K300 and K301. Of the two relays, K300 is normally closed (ramp in progress) and K301 normally open. When f(Ei) exceeds Ef, the comparator senses this condition and reverses the state of the relays, that is, K300 opens and K301 closes. The comparator also turns on the Tilt light for the time that f(Ei) exceeds Ef. K300 is connected between the current source and the summing point. Consequently, when K300 opens, ramping current is interrupted and no further ramping occurs. K301 is connected across the integrating capacitor. Consequently, whenever this relay closes, the ramp instantly resets, providing that the Repeat/Single switch is set to REPEAT. Note that the instant the ramp resets, f(Ei) will no longer exceed Ef. Hence K300 closes again and K301 opens, allowing another ramp to begin. If the Repeat/Single switch is set to SINGLE, the integrator capacitor will not be shorted when K301 closes. Hence, the ramp will not reset and K300 will remain open. The effect is the same as would be obtained by setting the Delay Mode switch to HOLD.

Whenever f(Ei) exceeds Ef, the relays switch as indicated in the preceding paragraph and the Tilt light turns on. It should be noted that, because f(Ei) always exceeds Ef if the scan ramp is allowed to reach its maximum value, the Tilt lamp turns on at the end of each scan. In the Repeat mode, the flash will be momentary. In the Single mode, the Tilt lamp will glow steadily to indicate the end of the scan. If the Delay Mode switch is set to DELAY, f(Ei) is simply Ei, and the Ef versus f(Ei) Comparator will cause the Tilt light to glow steadily whenever Ei exceeds Ef, that is, when the Initial Delay is set higher than the Final Delay.

DELAYED TRIGGER COMPARATOR

This comparator, which has as its inputs the time base ramp and a voltage picked off the Delay Trigger potentiometer, provides an output pulse which can be used in delayed trigger applications as explained in Section III. The pulse begins coincident with the crossover of the time base ramp over the voltage picked off the potentiometer and ends coincident with the end of the time base ramp as the resetting ramp crosses over the potentiometer voltage again.

MONOSTABLES

There are two monostables, each of which controls a gate. The high resolution monostable controls the high speed sampling bridge which acts as the gate when operating in the high resolution mode. The normal resolution mode monostable controls Q600, the field effect transistor which acts as the gate in the normal resolution mode, and which also functions as a pulse stretcher in the high resolution mode. Note that the output of both monostables is applied to a shaper which shifts the levels of the pulse as required by the

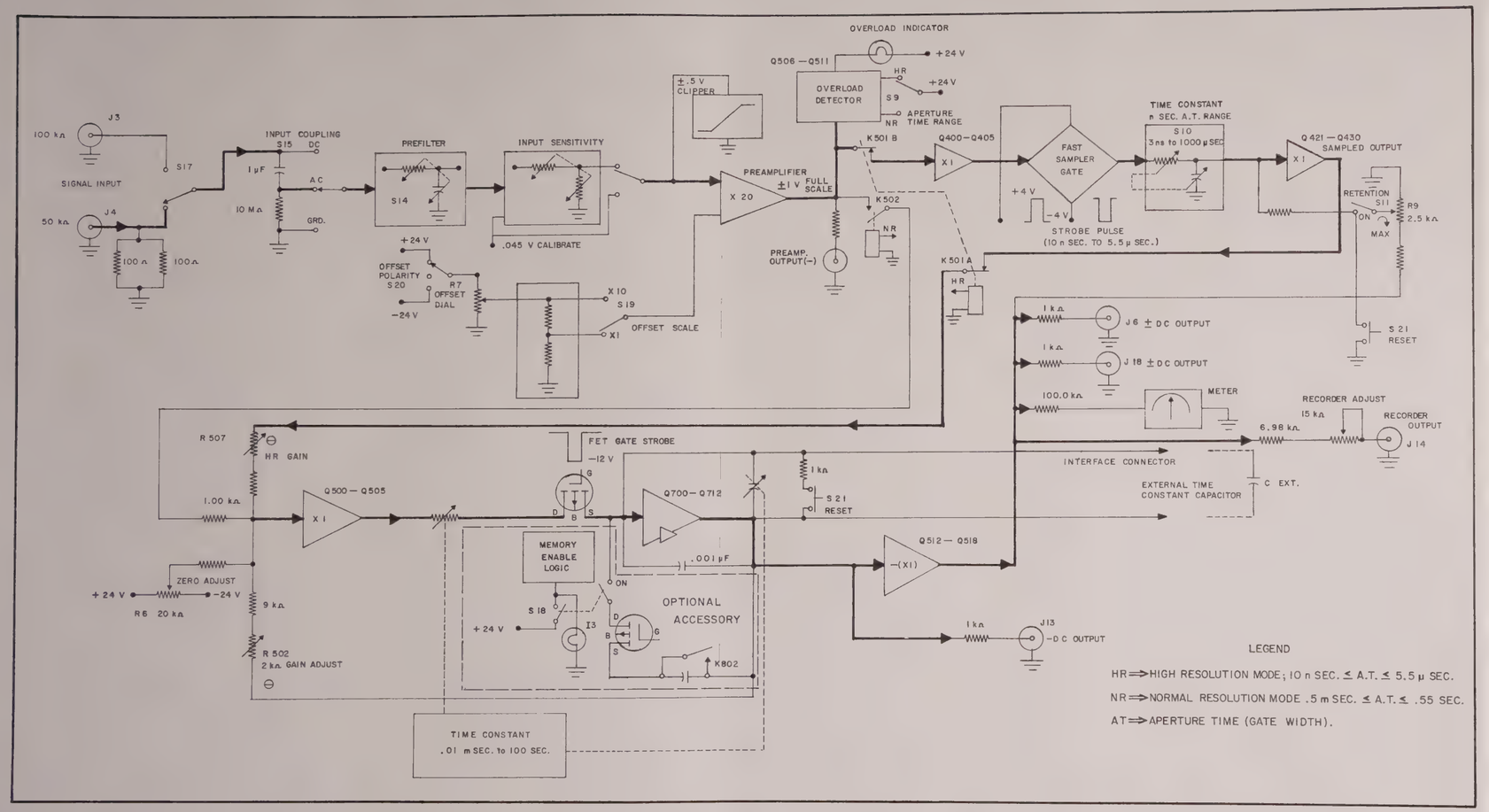


Figure IV-5. BLOCK DIAGRAM OF SIGNAL CHANNEL

gate. The pulses are also applied to a Gate Selector circuit which determines which monostable output will be supplied to the Gate Out jack. The Gate Selector circuit senses the position of the Aperture Time Range switch and so allows either the fast monostable output or the normal resolution monostable output to be supplied to the Gate Out jack, whichever is appropriate.

Note that the Gate Out pulse is also supplied to the logic gate which controls the Tilt monostable. This same gate samples the output of the time base control logic. Should the duration of the gate out pulse, and hence the duration of the aperture opening, extend beyond the time base interval, the monostable will be repeatedly fired and the Tilt light will flash. Note that the earlier discussed Tilt signal from the Ef versus f(Ei) Comparator bypasses the Tilt monostable. As a result, the Tilt light does not flash but instead glows steadily if f(Ei) exceeds Ef or if a single scan is completed.

4.5 SIGNAL CHANNEL

INTRODUCTION

Signal channel functioning is relatively straightforward, with the only complicating factor being the instrument's capability of transferring from the normal resolution mode to the high resolution mode and vice versa. In the following paragraphs, the signal channel is discussed from an organizational and functional point of view, with separate diagrams of that portion of the signal channel under consideration. Figure IV-5, a block diagram of the entire signal channel, is not discussed separately, but is provided as a handy reference for determining how the separate signal channels relate.

INPUT SIGNAL CHANNEL

Referring to Figure IV-6, a simplified schematic of the Input Signal Channel, note that the input signal is applied to either the 100 kΩ Input jack or to the 50 Ω Input jack. Input Selector switch S17 selects the appropriate signal and transmits it through 50 ohm cable to the Coupling switch, whose function is to determine whether the signal will be dc coupled (straight through), ac coupled (through 1 μF), or grounded. If the fifty ohm input is selected, the cable is terminated in fifty ohms via the "B" contacts of S17. For this reason, the signal source driving the fifty ohm input will always "see" a 50 ohm resistive load, independent of the selected coupling mode.

Prefilter switch S14 is inserted prior to any attenuation to provide a means of limiting the bandwidth of the input signal. The filter is, in principle, a single section, RC, low-pass filter, which provides an attenuation of 6 dB/octave beyond the cutoff or 3 dB corner frequency. The low pass filter is characterized by a 10,000 ohm series resistance with appropriate capacitive compensation for each switched filter position. Detailed RC values are shown on the corresponding schematic (page VIII-13).

Following filtering, the signal is attenuated by the Sensitivity switch (S16) to normalize all full scale inputs to 45 mV referred to the input of the Preamplifier. When the Sensitivity switch is in the CAL. position, the input signal is disconnected from the Preamplifier input and replaced by a fixed

45 mV ±0.2% calibrate dc level. Otherwise, the attenuator has a characteristic input impedance of 90 kΩ, thus providing the input jack with a 100 kΩ input impedance (10 kΩ prefilter plus 90 kΩ attenuator).

The input stage of the Preamplifier consists of a matched and balanced pair of source followers, Q1100A, which senses the attenuated input signal, and Q1100B, which subtracts out any "dialed in" offset voltage. It should be noted that the offset voltage does not "null" any dc level, but serves to introduce a variable common mode voltage, allowing the Preamplifier to amplify only the difference voltage. Diodes CR1102 and CR1103 limit input signals which exceed the dynamic range of the preamplifier. The biasing on the diodes is such that the input signals can be as great as ten times full scale before limiting occurs, a level commensurate with the dynamic range capabilities of the Preamplifier.

The preamplifier gain is nominally 20 (+26 dB), thus providing a 1 V output with a full scale input signal. The Preamplifier has a second output which is of opposite polarity but otherwise the same as the main output. This inverted output is connected to a rear panel jack through a nominal 300 ohm output impedance, which provides a pseudo current source when the output connector is terminated in 50 ohms.

NORMAL RESOLUTION MODE SIGNAL PROCESSING

Figure IV-7 shows the circuitry used to process signals in the "normal" resolution mode (Aperture Times from 0.5 µs to 0.55 s). Amplifiers A2 and A3, in conjunction with the MOSFET switch (Q600), constitute the forward loop of a "gated amplifier", that is, an amplifier which changes its output only when switch Q600 is conducting ("on"). Amplifier A2 is a unity gain buffer amplifier and A3 is a chopper-stabilized, high-gain amplifier. Because A3 is always connected as an integrator (1 nF minimum feedback capacitance), A3 integrates the current provided by amplifier A2 when the gate is conducting. Over the intervals when the gate is not conducting, the amplifier output "holds" at the level attained at the end of the preceding conduction period. As A3 "acquires" the input voltage (assuming the conduction time is small with respect to the loop time constant), the net applied voltage (current), as viewed from the output of A2, is reduced because of the negative feedback. The whole integrator loop exhibits a time domain response equivalent to that of a simple RC low pass filter whose time constant is the integrator's RC values modified by the closed loop gain. In this case, the gain is approximately ten (ratio of feedback to input resistances) with a corresponding increase in the loop time constant. Values of the equivalent time constant resistance and capacitance are given in Table III-2 (page III-23).

Amplifier A4 is a unity gain inverting amplifier whose only function is to provide correct polarity agreement between the input and output.

An overload indicating circuit (Q506-Q511) senses either a positive or negative preamplifier output signal and lights the Overload lamp. The overload criterion depends on the resolution mode. It is ten times full scale in the normal resolution mode and 3.5 times full scale in the high resolution mode.

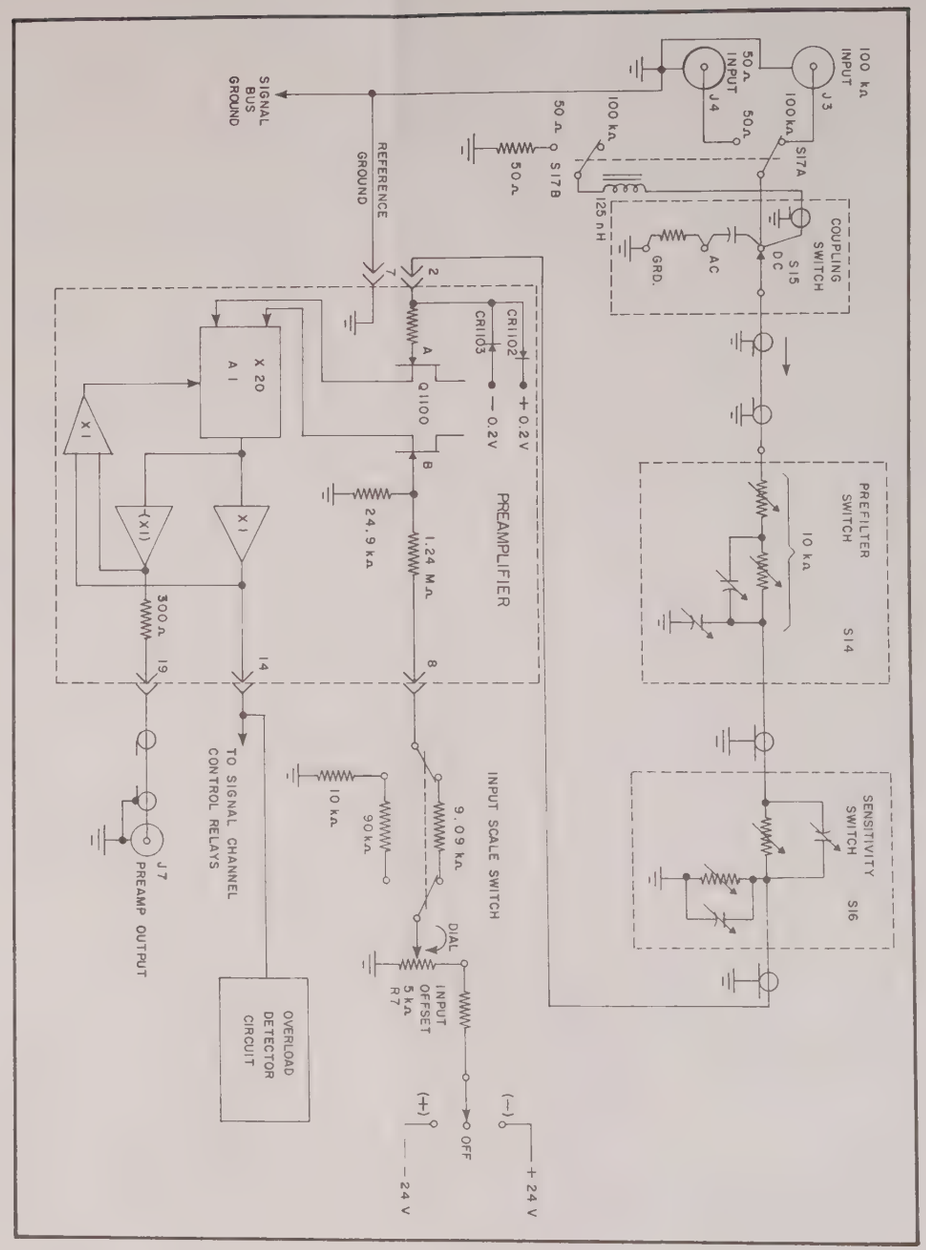


Figure IV-6. SIGNAL INPUT CHANNEL

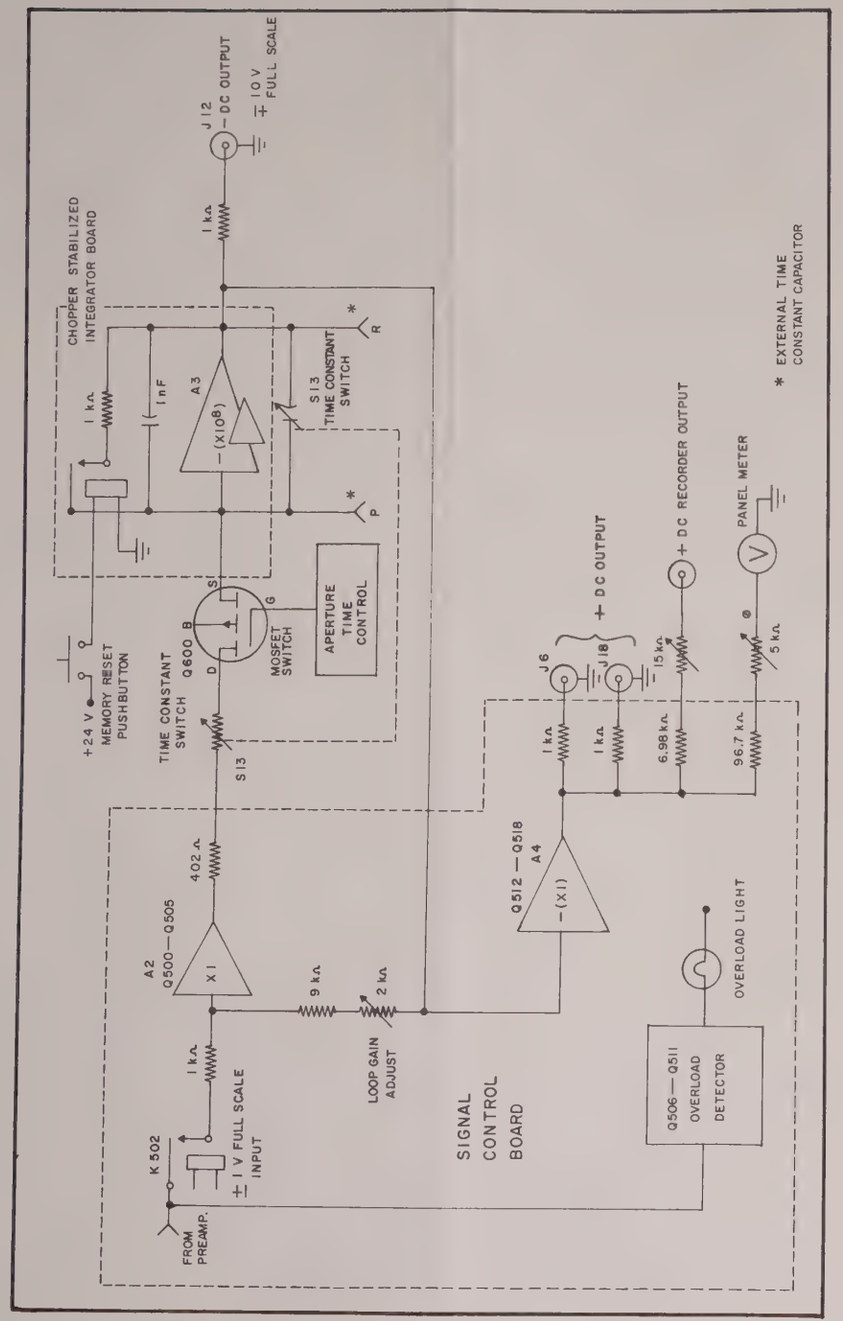


Figure IV-7. NORMAL RESOLUTION MODE SIGNAL PROCESSING

HIGH RESOLUTION MODE SIGNAL PROCESSING

Signal processing in the high resolution mode (10 ns through 5.5 µs) is similar to signal processing in the normal resolution mode, but differs considerably in implementation. As shown in Figure IV-9, the preamplifier output is routed through relay K501B to buffer amplifier A5, then sampled, averaged by a low pass filter, and buffered again. The sampled signal is then routed to the main gated integrator, which, in the high resolution mode, serves as a "signal stretcher". The stretch time, the actual time interval over which Q600 conducts with each repetition of the input signal, is either 10, 30, or 100 µs, according to the position of the Stretch Time switch. By intentionally making the effective time constant of the stretch time circuit long relative to the effective High Resolution Time Constant, the effective time constant of the entire signal processing channel may be increased well beyond R1C1. The equivalent circuit in Figure IV-8 illustrates this point.

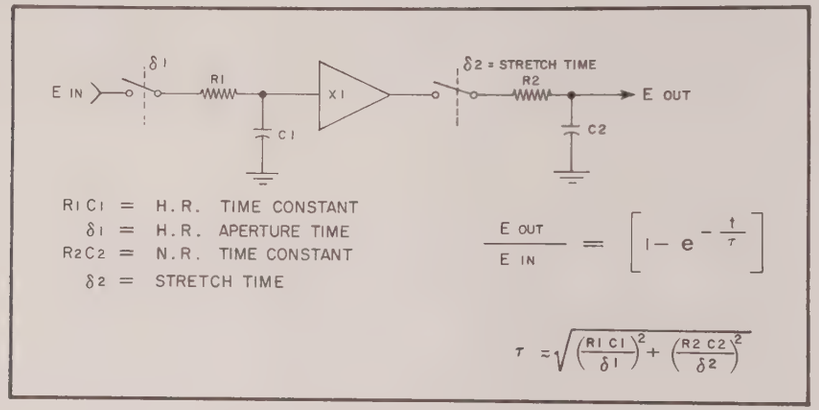


Figure IV-8. EQUIVALENT STRETCH TIME CIRCUIT

Because the sampling bridge circuitry does not have the extended holding time characteristic of the gated amplifier, it is possible for the sampled signal to partially decay over the stretch time interval. This would cause the output signal to be only partially averaged by the stretch circuit with a resulting large error. Referring again to Figure IV-9, note the positive feedback signal taken from the output and applied directly to the high resolution mode time constant filter. When optimally adjusted (positive loop gain of slightly less than unity), there will be no signal decay over the stretch time interval, with a resulting great improvement in the high resolution mode signal processing accuracy. This adjustment is provided by means of the front panel Retention control.

OUTPUTS

In both the normal and high resolution modes, the output of the Model 160 is in fact the output of the chopper stabilized integrator. However, because

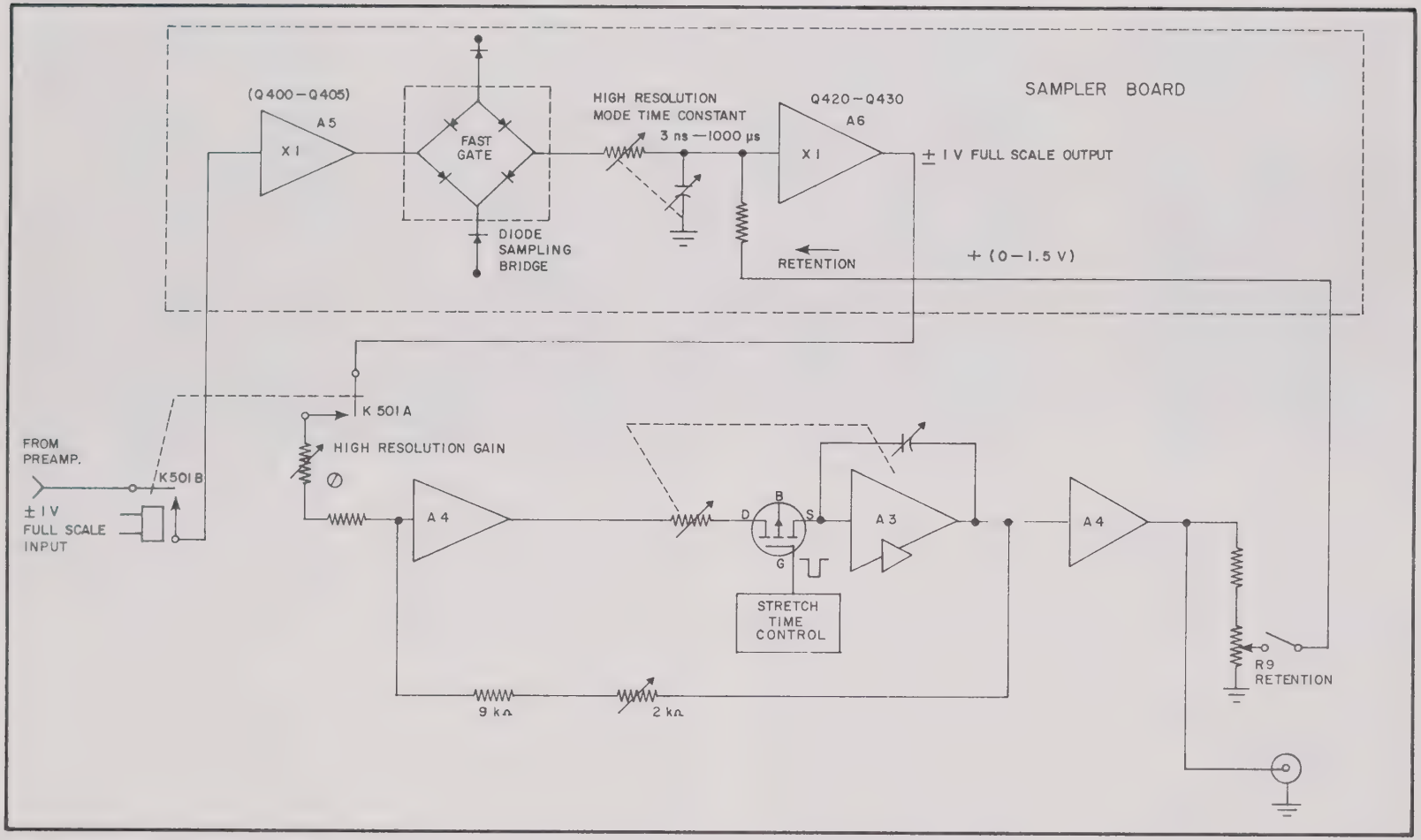


Figure IV-9. HIGH RESOLUTION MODE SIGNAL PROCESSING

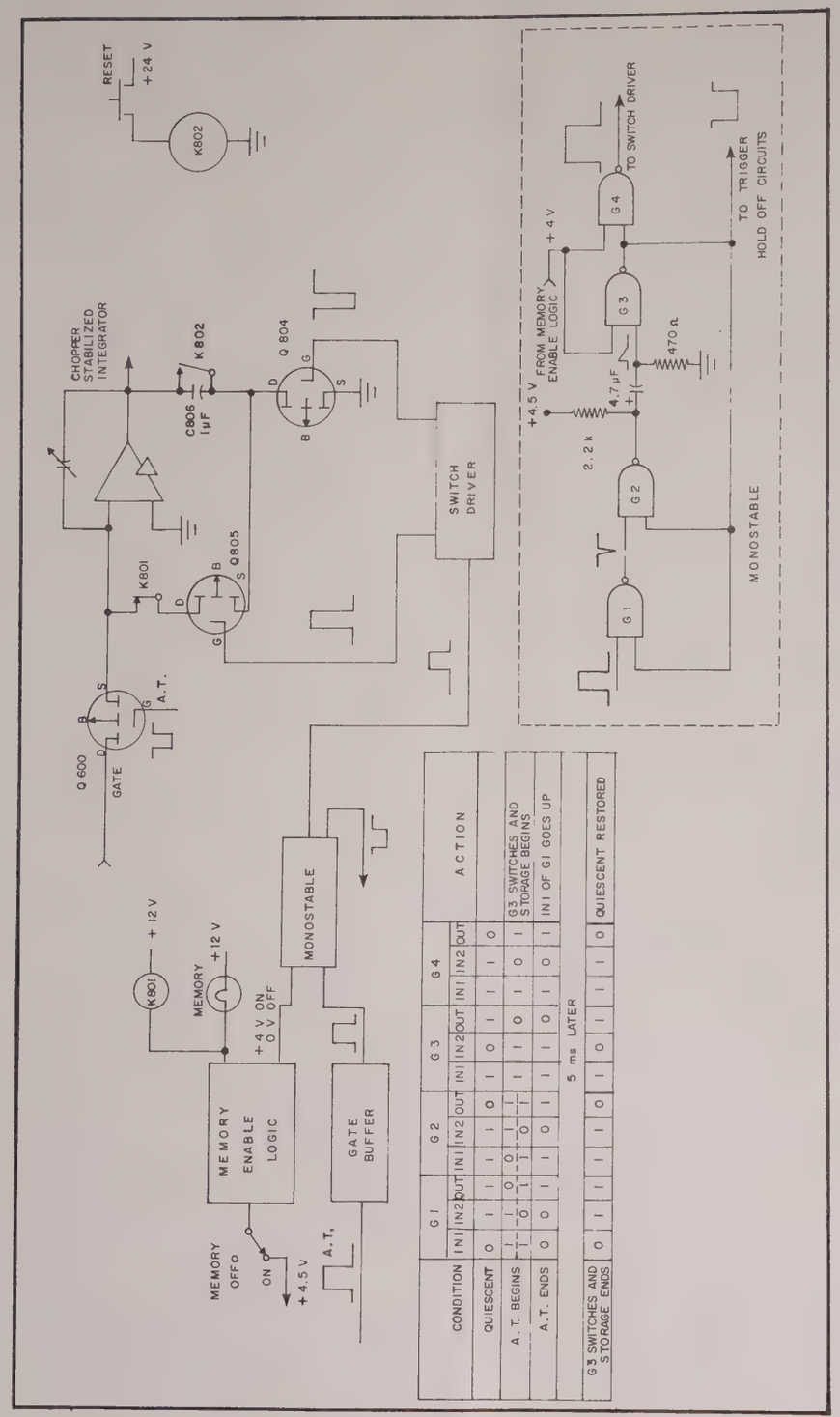


Figure IV-10. BLOCK DIAGRAM OF ANALOG STORAGE CIRCUITRY

this output is inverted relative to the input signal, an additional inverter is interposed between the chopper stabilized integrator and most of the instrument outputs. Three 1000 ohm BNC jack outputs are provided, two at the rear panel and one at the front panel. The front panel output is of the same polarity as the input signal, as is one of the rear panel outputs. However, the second rear panel BNC output jack is fed directly from the output of the chopper stabilized integrator, making the signal at that jack inverted. The meter is driven from the non-inverted signal line and so properly indicates the polarity of the input. Last is the recorder output, also the same polarity as the input. Note that the resistance of the recorder output can be varied from seven kilohms to approximately 22 kilohms by means of the associated control.

4.6 ANALOG STORAGE ACCESSORY

The analog storage accessory allows long hold times to be achieved when the instrument is operating with a short time constant. Ordinarily, short time constant holding times are degraded relative to long time constant holding times because of offset current at the input of the chopper stabilized integrator. Although this current is small, typically a few picoamperes, it can cause significant drift with low duty factors and short time constants. With a longer time constant, a larger capacitor is connected around the integrator and the drift between aperture intervals is reduced proportionally to the increase in capacitance. The limit in attainable improvement is reached when the capacitor leakage currents become larger than the offset current. Practically, there is no advantage in having a capacitor larger than about one microfarad.

The analog storage accessory implements its improved holding time by charging a one microfarad capacitor to the integrator output voltage each time the aperture opens. When the aperture closes, and for the duration between aperture openings, the capacitor is connected between the output of the integrator and its summing junction. Thus, for small time constants, the holding time achieved is the same as if the time constant capacitor were one microfarad instead of the small value (minimum of one nanofarad) associated with the short time constant. Inasmuch as the capacitor is connected between the integrator output and ground during the aperture opening, as opposed to being connected between the integrator output and the summing junction, the analog storage capacitor has no effect on the operating time constant. With the exception of the improved holding time, the instrument characteristics are unaltered.

Referring to Figure IV-10, a block diagram of the Analog Storage circuitry, note C806, the analog storage capacitor. Associated with C806 are field effect transistors Q804 and Q805. These transistors are arranged such that at any time, one, and only one, is conducting. When Q804 conducts, the analog storage capacitor is connected between the output of the integrator and ground. When Q805 conducts, the capacitor is connected between the output of the integrator and the summing point. Reed relay K801 is open when the analog memory is not in use, thereby preventing the capacitor from being connected around the integrator, even though Q805 is in the conducting state. Because Q804 does not conduct when the analog storage accessory is not in use, the analog storage capacitor is effectively disconnected from the non-

storage circuitry.

When the memory is turned on, the Memory Enable Logic circuit supplies current to K801, thereby connecting the analog storage capacitor to the summing point of the integrator. Additionally, the Memory Enable Logic circuit turns on the Memory light and supplies an enable level to the monostable, which generates the 5 ms storage pulse.

In the quiescent state, that is, with the Memory on but no aperture opening in progress, the monostable is in the enabled state, but will not be generating a pulse. The switch driver circuit will be holding Q805 in conduction and Q804 in cutoff, and the analog storage capacitor will be connected between the output and summing junction of the integrator.

Assume a trigger is applied, with the resulting subsequent generation of a time base ramp. Some time after initiation of the time base ramp, a gate pulse (or stretch pulse if the instrument is operating in the high resolution mode) is applied to Q600. A positive pulse, coincident with the gate pulse, is applied to the input of the Analog Storage Gate Buffer. This same pulse appears at the output of the buffer, from where it is applied to the monostable. Because the Memory Enable Logic will be providing an enable output to the monostable, it can be triggered and the monostable produces a 5 ms pulse which is routed to the switch driver. For the duration of the 5 ms pulse, Q804 conducts and Q805 does not. Consequently, any change in the integrator output over the aperture interval (it is assumed that the aperture interval is shorter than the 5 ms storage pulse) will cause an equal change in the voltage across the analog storage capacitor. At the end of the 5 ms storage period, Q805 and Q804 revert to their quiescent state and the analog storage capacitor is again connected around the integrator.

Figure IV-10 also contains a separate "sub-diagram" showing the "monostable" in greater detail. Note that it comprises several NAND gates. A truth table is provided to show how the monostable function is achieved. Quiescently, the output of G1 is up while that of G2 is down. When the gate pulse is applied, both of these gates change state. The positive transition at the output of G2 is coupled to G3, causing that gate as well as gate G4 to change state. Feedback is applied from the output of G3 to the inputs of G1 and G2. This feedback "holds" G2 in the changed state but returns G1 to its quiescent state. Thus the negative transition at the output of G1 marking the arrival of the gate pulse is transitory. Gates G3 and G4 remain in their changed state for a time determined by the RC network between the output of G2 and the input of G3. After 5 ms the capacitor discharges sufficiently for input two of G3 to again approach ground potential, allowing this gate and G4 to revert to their original state. The feedback to G2 then forces G2 to resume its original state. This feedback also establishes the quiescent input conditions at G1 (although the output of this gate was already restored).

Note that the monostable enable level from the Memory Enable Logic is applied to G3 and G4 in such a manner as to prevent these gates from changing state if the Analog Memory switch is not set to ON, this regardless of the effects of pulses applied to G1.

As a final note, Relay K802 allows the analog storage capacitor to be discharged when the Reset pushbutton is depressed.

4.7 CIRCUIT DESCRIPTION

INTRODUCTION

Most of the Model 160 circuitry is located on the plug-in circuit boards. Schematics are located in Section VIII, with a separate schematic provided for each circuit board. The remainder of this section consists of a series of circuit descriptions, with each board treated separately. It will usually be advantageous to refer to the corresponding schematic when reading the circuit description. Each schematic folds out for convenience.

TRIGGER BOARD (page VIII-2)

Trigger Input Detector

Referring to the Trigger Board schematic on page VIII-2, note that the input triggers are applied to the Trigger Input Detector circuit, which comprises transistors Q100, Q102, Q103, and Q104, along with their associated components. This circuit is a simple tunnel diode switching circuit of the type described in subsection 4.3. Considering the function of the individual components, Q100 and Q104 are input emitter followers, with the input trigger being applied to the base of Q100 and the trigger comparison voltage from the Threshold potentiometer being applied to the base of Q104. These emitter followers drive the emitter coupled pair, Q102 and Q103. One of these transistors conducts and the other is cut off; the determination as to which conducts and which does not depends on the setting of the Threshold control and on the applied input signal. Each time the trigger pulse crosses over the threshold voltage, the conducting transistor cuts off and the cut off transistor conducts, causing tunnel diode CR103 to switch as discussed in subsection 4.3 The resultant output is a pulse whose duration is the same as that of the applied trigger. Because of the extreme speed of the tunnel diode switch, even relatively "slow" input triggers will result in sharp clean output pulses from the Trigger Input Detector circuit.

Trigger Shaper

The next circuit is the Trigger Shaper, which accepts the output from the Trigger Input Detector circuit and adjusts it to the proper dc levels required by the NAND gate logic circuitry which follows. Transistors Q105 and Q106 constitute an emitter coupled pair. The diodes in the collector circuits limit the output swing to the levels shown on the schematics. The collector signals are applied to the output emitter followers, Q107 and Q108, which drive the trigger logic circuitry.

Trigger Logic

The reader is referred to "TRIGGER CIRCUITS", page IV-4, for a description of the trigger logic functioning.

External Time Base Buffer Amplifier

This "amplifier", which comprises Q109 and Q110 arranged in a complementary emitter follower configuration, acts as a buffer between an externally de-

rived time base signal and the other internal circuits. Note that the output of this circuit is applied to contacts of K100. When the instrument is operating in the Internal Time Base mode, K100 is not energized, and the internally developed Time Base ramp is applied to the Time Base Output Buffer Amplifier at the base of Q111 and to the Delayed Trigger circuitry at the base of Q113. When operating in the External Time Base mode, a relay, K201 on the Time Base board, interrupts the output of the internal time base generator. At the same time, K100, now energized, applies the output of the External Time Base Buffer Amplifier to the following circuits.

Time Base Output Buffer Amplifier

This circuit, Q111-Q112, is another complementary emitter follower. It acts as a buffer between the time base ramp and the Reference Time Base Output jack, J9. When operating in the Internal Time Base mode, the signal applied to the base of Q111 is simply the time base ramp developed by the Time Base Generator (schematic on page VIII-3). When operating in the External Time Base mode, the input signal is the output of the External Time Base Buffer Amplifier, Q109-Q110.

Delayed Trigger Circuitry

Besides being applied to the Time Base Output Buffer Amplifier, the Time Base signal, either internally or externally derived, is applied to the input stage of the Delayed Trigger circuitry, Q113 through Q120. This circuit in turn can be considered as comprising three separate circuits. Q113 through Q117 constitute a tunnel-diode fast-switching stage similar to that employed in the Trigger Input Detector. The principle difference between the two being that, whereas the Trigger Detector compared the trigger signal with the Threshold voltage, the Delayed Trigger circuit compares the time base ramp either with the dc voltage picked off the Trigger Delay potentiometer or with f(Ei) (sum of Scan and Initial Delay voltages), as determined by the position of the Trigger Delay DIAL/SCAN switch. The circuit (Q113 through Q117) produces a negative pedestal which begins coincident with the positive going crossover and ends with the reset crossover. With the DIAL/SCAN switch set to DIAL, the position of the pedestal relative to the trigger time is determined by the setting of the Trigger Delay dial. With the switch set to SCAN, the position of the pedestal will automatically scan in step with the ramping f(Ei) voltage. In either case, the pedestal is applied to amplifier stage Q118-Q119, and from there to inverter Q120, which supplies the now positive pedestal to the front panel Delayed Trigger Output jack.

TIME BASE BOARD (page VIII-3)

Time Base Generator

Referring to the schematic on page VIII-3, note that the Time Base Generator (Q214 through Q219) is an operational amplifier connected as an integrator-type ramp generator. Field-effect transistors, Q214 and Q215, are used at the input to achieve a high input impedance, thereby assuring that input offset currents will not degrade the linearity of the time base ramps. Q216 and Q217 constitute an emitter coupled amplifier pair which provides additional amplification. A complementary emitter follower, Q218-Q219, provides a low

output impedance with diodes CR218 and CR219 serving to compensate the emitter base drops of Q218 and Q219.

The amplifier summing junction is at the gate of Q214 with the gate of Q215 serving as the reference or non-inverting input. When the circuit is quiescent, that is, when a ramp is not in progress, diode CR216 is forward biased by the Time Base Control Logic (a detailed description of the functioning of this logic can be found under TIME BASE GENERATOR AND CONTROL CIRCUITS, page IV-5). Because of the resulting positive input from a low source resistance, the ramp generator output is driven negative. However, diode CR215, being forward biased by the negative output, prevents the output from going more than a fraction of a volt negative. When a ramp is in progress, CR216 is reverse biased, and the output ramps positively at the rate determined by the current supplied to the summing junction through R272 and by the magnitude of the integrating capacitance.

As the Time Base Range switch is rotated through its various positions, both the ramping current and the capacitance are changed as required to achieve the proper ramping rate. The details of how this is accomplished can be determined by referring to the schematic of instrument switches located on page VIII-14. Note that one integrating capacitor, C215, is located on the circuit board. Other integrating capacitors are located on the switch, allowing them to be switched in parallel with C215 in the combination appropriate to the selected Time Base range. Reed relay K200, which is located on the circuit board, allows the line going to the switch mounted capacitors to be disconnected from the board circuitry on the six "fastest" Time Base Range switch positions. In these positions, C215 alone functions as the feedback capacitor. By disconnecting the line to the switch, the stray line capacitance cannot affect the time base accuracy.

Time Base Generator Control Logic

The reader is referred to TIME BASE GENERATOR AND CONTROL CIRCUITS, page IV-5.

Time Base Versus E_f Comparator

This circuit is basically a fast tunnel diode switching circuit of the type discussed in subsection 4.3. The Time Base ramp is applied to one input at the base of Q200 while E_f, the voltage picked off the Final Delay dial, is applied to the other input at the base of Q201. When the ascending ramp crosses over the dialed voltage, the tunnel diode switches as shown on the schematic. However, because the output of this circuit is fed to the control logic to reset the ramp generator, the crossover is momentary, and the output of the comparator is a fast negative transient.

Transistor Q202 is a constant current source for the comparator input pair and emitter-coupled pair Q203-Q204 provides additional gain. An emitter follower output stage, Q205, is used to achieve a low output impedance.

Time Base Versus Zero Comparator

This circuit is identical to the Time Base Versus E_f Comparator. Transistor

Q208 serves as a constant current source for the input pair, Q206-Q207. Pair Q209-Q210 furnishes additional gain and Q211 is an output emitter follower. The circuit compares the time base ramp, which is applied to Q206, with the ground level (zero) at the base of Q207. Consequently, the output of the comparator is down for the duration of the time base, allowing it to be used to inhibit further triggering over the time base active interval.

E_f Buffer Amplifier

The voltage picked off the Final Delay potentiometer is not directly applied to the various circuits where it is used. Instead, it is routed through a complementary emitter follower stage, Q212-Q213, to prevent the potentiometer from being loaded.

Time Base Versus f(Ei) Comparator

This comparator is much like the other two comparators on this circuit board except that it has an additional output stage to provide complementary outputs. The outputs change state when the time base ramp crosses over f(Ei), which may be a fixed (Delay Mode) or changing slowly (Scan Mode). The outputs resume their quiescent levels when the resetting time base ramp crosses over f(Ei) again. Diodes CR225 through CR230 establish the output levels at their proper values.

In an analogous manner to the other comparators, Q222 is a current source for the input pair, Q220 and Q221. Tunnel diode CR221 provides fast switching, and pair Q223-Q224 furnishes additional gain. Emitter followers Q225 and Q226 provide a low output impedance to the following circuits, the monostables which control the two gates.

INTEGRATOR GATE CONTROL BOARD (page VIII-4)

Normal Resolution Monostable

The Normal Resolution Monostable, Q604 through Q608, is triggered by the pedestal generated by the Time Base Versus f(Ei) Comparator located on the Time Base board. The positive going leading edge of the pedestal is coupled through C609 to the input of the monostable. The monostable generates the pulse which, after shaping by the Q601-Q602 circuit, opens the normal resolution gate, Q600, for an interval equal to the selected aperture time. The monostable output is also routed to logic circuits of the Gate Selector circuit and to the Trigger Inhibit logic circuits (Time Base Board).

Consider one cycle of the monostable in detail. Quiescently Q607 is cut off and its collector is established at +15 V by the R622-R624 divider. Complementary emitter follower Q604-Q608 establishes the voltage applied to the timing capacitors (parallel combination of C612, C613, and the capacitor selected by the Aperture Time switch) at +15 V as well. Current source Q613 supplies current to Q605, holding that transistor in saturation. Its collector voltage of about +1.2 V is applied to emitter follower Q606, with a resultant monostable output voltage at the emitter of Q606 of 0 V. Note the feedback from the output of the monostable through diode CR627 to the monostable input at the base of Q607. In the quiescent state, this feedback is

effectively open because of the high resistance of diode CR627 (ground potential is applied to both its anode and cathode).

Assume a trigger pedestal is applied. It will be differentiated by the coupling network and a positive transient will be applied to the base of Q607, biasing that transistor into conduction. The amplified and inverted transient appears at the collector of Q607 and is applied by the Q604-Q608 emitter follower stage to the timing capacitance, which couples the negative transient to the base of Q605, cutting that transistor off. When Q605 cuts off, its collector voltage goes to about +4.5 V as established by resistor network R629-R630, and emitter follower Q606 follows. Thus the monostable output rises to +4 V. This level forward biases CR627, and the positive level is applied to Q607, holding that transistor in conduction. Because of the feedback, the circuit is "held" in the switched state. However, it cannot remain switched indefinitely. Current source Q613 continues to supply current to the timing capacitors, charging them at the rate of i/C volts per second, where "i" is the current supplied by Q613, and "C" is the magnitude of the timing capacitance. When the rising voltage at the base of Q605 reaches 1.2 V, the transistor resumes conduction. It immediately goes into saturation; its collector goes to +0.6 V and emitter follower Q606 re-establishes the monostable output at 0 V. As soon as the output returns to zero, CR627 stops conducting and input transistor Q607 is cut off by ground applied to its base through R623, thereby restoring the quiescent state.

Note that the Aperture Time Range switch connects different capacitors in parallel with C612 and C613, and that the Aperture Time Multiplier varies the current supplied by Q613 by varying the resistance of R5B. Trim-potentiometers R653 and R650 allow calibration of the minimum and maximum current supplied by Q613.

The Stretch Time switch also determines the timing capacitance of the Normal Resolution Mode monostable. Switch S9 shorts out R5B when operating in the high resolution mode, with the effect that the charging current provided by Q613 is independent of the setting of the Aperture Time Multiplier. The stretch time is determined by the timing capacitance only.

NR Gate And Shaper

From the emitter of Q606, the normal resolution monostable output pulse is applied to diode CR608, which routes the pulse to the shaper input at the base of Q602 when the instrument is operating in the External or Recurrent Trigger mode. The shaper comprises emitter coupled pair Q601-Q602 and their associated components. Quiescently, Q602 conducts and Q601 does not, establishing the collector of Q602 at approximately +0.6 V and the collector of Q601 at about -12 V. Because the collector of Q602 drives the gate of Q600, the Normal Resolution Gate, Q600 will be in cutoff. When the monostable output pulse is applied to the base of Q602, the pair switches, and the gate of Q600 goes to -12 V, biasing the gate into conduction and allowing that portion of the input signal which is applied over the gate open interval to reach the Chopper Stabilized Integrator. Note that a small portion of the complementary signal at the collector of Q601 is coupled through C601 to the drain of Q600. This signal compensates high frequency offset effects in Q600.

In addition to the monostable input to the shaper through CR608, two other inputs are provided through CR607 and CR606. The input through CR607 locks the gate into conduction when the Trigger Mode switch is set to CONTINUOUS. The CR606 input allows the gate to be contolled by externally derived timing signals applied to J12, the External Gate Input jack. Transistor Q603 buffers the external gate timing signals.

Gate Selector

The Gate Selector circuit, Q614, Q615, and the three associated NAND gates, determines whether the pulse supplied to the front panel Gate Out jack will be the normal resolution mode monostable output or the high resolution mode monostable output. It also supplies an output to the Tilt Logic to assure that this circuitry will be sampling the proper gate pulse for detection of the end of time base overlap "tilt" condition.

Both Q614 and Q615 are simple inverters. When the instrument is operating in the normal resolution mode, Q614 is shut off and Q615 conducts. In the high resolution mode the situation is reversed. In any case, each of these transistors drives a NAND Gate, one of which receives the normal resolution mode monostable output pulse and the other the high resolution "strobe" pulse. According to which transistor is conducting, one gate or the other supplies a pulse to the following gate (G3 in Figure IV-11), which routes the pulse to the following circuits. Figure IV-11 also includes truth tables showing the circuit operation in both the normal and high resolution modes.

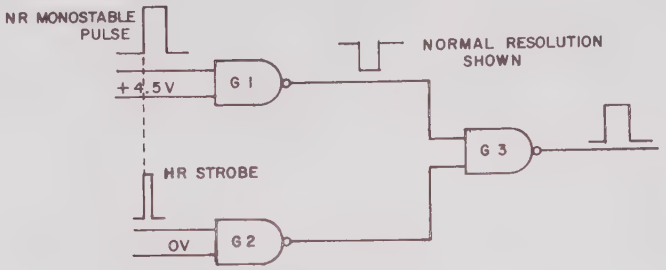
Gate Output Buffer

Whichever of the two gate pulses is routed through the Gate Selector is applied to Q616, an output emitter follower which buffers the gate pulse prior to supplying it to the Gate Output jack.

Tilt Logic Circuitry

The input stage of the Tilt Logic circuit is the NAND gate that uses leads 8, 9, and 10 of the integrated circuit located on the Integrator Gate Control Board. Note that the gate pulse output of the Gate Selector is applied to one input and that the output of the Time Base Generator Control Logic is applied to the second input of the gate. In the quiescent state, the down level at pin 10 of the integrated circuit forces the gate output up. When a ramp is in progress, the down level at pin 9 forces the output to be up; a gate pulse occurring when the time base ramp is in progress will have no effect because of the down level at pin 9. However, if a pulse extends beyond the end of the time base period, both pins 9 and 10 will be up and the output will go down. This negative transistion is coupled through capacitor C616 to the input of the Tilt monostable, Q609-Q610. The monostable produces a negative pulse which biases Q611 into conduction; the Tilt lamp turns on. Assuming the trigger repetition rate is high relative to the period of the Tilt monostable (the usual case), the monostable will be retriggered as soon as it recovers. This process repeats with the effect that the Tilt lamp flashes repetitively.

Note that the Tilt Lamp driver transistor, Q611, has two inputs, one being



NORMAL RESOLUTION MODE

CONDITION	G 1			G 2			G 3			ACTION
	IN 1	IN 2	OUT	IN 1	IN 2	OUT	IN 1	IN 2	OUT	
QUIESCENT	0	1	1	0	0	1	1	1	0	
BOTH PULSES BEGIN	1	1	0	1	0	1	0	1	1	OUTPUT PULSE COINCIDENT WITH NR MONOSTABLE PULSE
HR STROBE ENDS	1	1	0	0	0	1	0	1	1	
NR PULSE ENDS	0	1	1	0	0	1	1	1	0	

HIGH RESOLUTION MODE

CONDITION	G 1			G 2			G 3			ACTION
	IN 1	IN 2	OUT	IN 1	IN 2	OUT	IN 1	IN 2	OUT	
QUIESCENT	0	0	1	0	1	1	1	1	0	
BOTH PULSES BEGIN	1	0	1	1	1	0	1	0	1	OUTPUT PULSE COINCIDENT WITH HR STROBE PULSE
HR STROBE ENDS	1	0	1	0	1	1	1	1	0	
NR PULSE ENDS	0	0	1	0	1	1	1	1	0	

Figure IV-11. GATE SELECTOR LOGIC

the just discussed output of the Tilt monostable and the second being the output of the E_f Versus f(Ei) Comparator. This second input can be activated in two different ways. First, the Tilt indicator lights if the initial delay exceeds the final delay. Second, when operating in the scan mode under single sweep conditions, it lights and glows steadily to indicate the end of a scan.

Tilt Monostable Cycle

Quiescently, Q609 is held cut off by the positive voltage applied through R635. Q610 is held in saturation by the negative potential applied through R638, establishing a -1 V potential at the collector of Q610. When the output of the Tilt gate goes down, the negative transient is coupled through C616 and diode CR615 to the base of Q609, cutting that transistor off and allowing the collector voltage to drop to approximately -12 V, as established by R639 and R640. Feedback applied through R636 to the input of the mono-

stable sustains conduction in Q609. After approximately half a second, the current supplied by R638 charges C617 sufficiently for Q610 to be biased into conduction again and the transistor immediately saturates, restoring the output to the quiescent state. The positive potential applied through R635 regains control of the input transistor with the decrease in negative feedback through R636, cutting the transistor off and ending the cycle.

SCAN/PULSE BOARD (page VIII-5)

Delay Scan Generator

This circuit, like the time base generator, is basically an operational amplifier connected as an integrator-type ramp generator. Referring to the schematic on page VIII-5, note that the scan generator comprises transistors Q300 through Q306, along with their associated components. Considering the function of these elements in greater detail, transistor Q300 is a constant current source for the input pair Q301-Q302. An insulated gate type field effect transistor (Q301) is used at the input to assure that input leakage currents do not degrade the very slow ramps, which can be as slow as 1000 minutes full scale. Q302 is the same type transistor as Q301 and has matching characteristics to achieve good temperature tracking. Trimpotentiometer R317 allows zeroing of the ramp "base line". Transistors Q303 through Q305 constitute a high gain amplifier stage which drives the output emitter follower, Q306. There are three integrating capacitors, those being C304, which is located on the board, and C010 and C011, which are mounted external to the board. Note that the Scan Reset pushbutton shorts out these capacitors. Ramping current is supplied to the summing junction from resistors mounted on the Scan Period switch. The output of the Scan Generator is routed to the Delay Mode switch, from where it is applied to the Delay Scan Buffer in the Scan and Hold Modes.

Delay Scan Buffer

As shown on the schematic, the Delay Scan Buffer is an integrated circuit type operational amplifier connected as a simple gain-of-one inverter. An emitter follower, Q308, is used to lower the output impedance and increase the output current capability of the amplifier. Transistor Q307 is a simple emitter follower type "regulator" which has the -12 V power supply level as its input and which provides regulated -6 V power to the integrated circuit. Note that the voltage picked off the Initial Delay potentiometer is also applied to the input of the amplifier. Thus the initial delay voltage and the scan voltage are summed as explained in the block diagram discussion under TIME BASE VERSUS f(Ei) COMPARATOR on page IV-7.

Ef Versus f(Ei) Comparator

Unlike the other comparators in the Model 160, this one does not incorporate tunnel diodes to achieve a high switching speed. As the main purpose of this comparator is to control the Scan Ramp Generator, there is no need for high speed. Considering the circuit in detail, note that Q311 is a current source for the input pair, Q310 and Q313. The buffered final delay voltage from the Final Delay potentiometer is applied to the base of Q313, while a fraction of f(Ei), the sum of the initial delay and scan voltages, is applied to the base

of Q310. When f(Ei) is less than E_f, the normal state, K300 is energized (current supplied by Q309) and K301 is not energized (Q314 is cut off). When f(Ei) exceeds E_f, the circuit switches. As a result, K300 is de-energized and K301 energized. A detailed discussion of how these relays control the scan generator is found in the block diagram discussions. Note that Q315 senses the state of the comparator and provides an output to the Tilt circuit to achieve the appropriate tilt indications as discussed on the preceding page.

High Resolution Monostable

The high resolution monostable, Q316 through Q323, produces the very fast strobe pulses which unlock the fast gate. Special features employed to achieve the required speed include a non-saturating design and the use of reed relays to switch the timing capacitors. By using relays located on the board, the stray capacitance of the lines going to and from the Aperture Range switch cannot affect the circuit's functioning.

Transistors Q316 and Q319 form a differential amplifier pair. Quiescently, the base of Q316 is at a higher potential than the base of Q319 due to the bias voltages supplied by CR317 and CR318. Consequently, Q316 is conducting while Q319 is cut off. Emitter follower Q318 applies the collector potential to the timing capacitors. Transistors Q320 through Q322 do not contribute to the monostable action. Instead, they shape the monostable output from the collector of Q319 to the levels required to drive the following circuits.

Consider one cycle in detail. The negative leading edge of the Delay Comparator output is coupled through capacitor C319 to the base of Q316, tending to cut off that transistor. As the base and emitter of Q316 are driven more negative, Q319 becomes increasingly forward biased and begins conducting some of the current supplied by Q317. As a result, the collector voltage of Q316 is driven more positive, and, when coupled through emitter follower Q318, drives the base of Q319 further positive, causing Q319 to demand still more of the Q317 current. Thus, the common emitter circuit of Q316-Q319 holds Q316 off as long as Q319 conducts. Q319 would continue to conduct indefinitely if it were not for the circuit's second current source, Q323. Note that the positive transition at the base of Q319 reverse biases diode CR318, removing the shunt path for the current supplied by Q323; this current is then available for charging the timing capacitors. The voltage at the base of Q319 ramps negatively at the rate of i/C volts per second ("C" is the timing capacitance and "i" is the Q323 collector current). When the voltage reaches approximately -12.5 V, CR318 begins conducting and Q319 cuts off. As Q319 cuts off, Q316 begins conducting again, restoring the quiescent state.

As is the case with the normal resolution monostable, the charging current is determined by a potentiometer (R5A) operated by the Aperture Time Multiplier dial.

Diodes CR319 and CR320 clip the monostable output signal and so limit the swing to approximately ±0.5 V. This signal is applied to the shaper at the base of Q320. Q321 is a current source for the Q320-Q322 pair.

SAMPLER BOARD (page VIII-6)

Input Buffer Amplifier

The Input Buffer Amplifier is a high-speed, non-inverting, operational amplifier with a gain of one. Referring to the schematic on page VIII-6, note that the base of Q400 serves as the non-inverting input while the base of Q403 is the summing point. Transistors Q400 through Q403 constitute a high gain stage and complementary emitter followers Q404 and Q405 furnish a low output impedance. Note that 100% feedback is taken from the output and applied to the base of Q403 to establish the gain at one.

At low frequencies the emitters of Q400 and Q403 are essentially shorted together by L401, which influences the circuit at high frequencies only. Emitter follower Q401 establishes the same voltage at the collector of Q400 as exists at the collector of Q403. Diodes CR401 through CR413 establish the proper dc levels throughout the amplifier and compensate the emitter base drops of Q404 and Q405. The output of the Input Buffer Amplifier is routed through contacts of the Test Mode switch, which is located on the printed circuit board, to the sampling diode bridge.

Gate Shaper

The complementary output of the high speed monostable is applied to the Gate Shaper circuit (Q406-Q407), which consists of two common base amplifiers. Both transistors drive the Gate Strobe circuit for additional shaping prior to application to the diode sampling bridge. In addition, they drive the buffer amplifier which precedes the Tilt circuit.

Pre-gate Selector Buffer

This circuit, Q408, Q409, and Q410, consists of an emitter coupled pair followed by an emitter follower. Its purpose is to provide buffering between the outputs of the gate shaper and the Gate Selector circuit (Integrator Gate Board).

Note that the signal(s) are intentionally degraded (poorer rise time) by R428 and R429, so as not to limit the bandwidth of shaper stages Q406 and Q407. This degradation of the Pre-Gate Selector output does result in a time delay of about 30 ns and an inherent "stretching" of the width of the signal when viewed at the GATE OUT front panel jack.

Gate Strobe Shaper and Sampling Bridge

Prior to application to the Sampling Bridge, the high speed gate pulse output of the Gate Shaper is applied to the Gate Strobe Shaper, which consists of current sources Q412, Q418, and Q419, amplifiers Q411 and Q417, and emitter followers Q414 and Q416. This circuit acts through diodes CR412 and CR417 to control the Sampling Bridge (diodes CR410, CR411, CR415, and CR416). The Sampling Bridge Gate opens for the selected high resolution aperture time when the gate pulse is applied. Quiescently, negative four volts is applied to the junction of CR410 and CR415, reverse biasing both diodes. At the same time, positive four volts is applied to the junction of CR411 and CR416, re-

verse biasing those diodes as well. With all diodes reverse biased, there is no conduction through the bridge and the output signal of the Input Buffer Amplifier does not get through.

When a gate pulse is applied, the emitter voltage of Q414 rises to +4 V while that of Q416 drops to -4 V. As a result, diodes CR412 and CR417 become reverse biased, and, for the duration of the applied pulse, the bridge is effectively isolated from the "drive" circuitry. With CR412 and CR417 reverse biased, the bridge conducts; current from Q413 forward biases CR410 and CR415, and current from Q415 forward biases CR411 and CR416. Thus, for the duration of the gate pulse, the signal at the output of the Input Buffer Amplifier can pass through the bridge; in effect, the signal is sampled for the duration of the selected aperture time.

The output of the bridge is applied to the high resolution time constant circuits and to the Output Buffer Amplifier. Note that the time constant circuits consist of a series of RC networks with reed switches used to do the actual switching. By having the front panel time constant switch operate relays instead of directly switching the filter components, the stray capacitance of the wiring to and from the switch cannot affect the filtering.

Output Buffer Amplifier

This amplifier buffers the sampled signal prior to routing it to the signal control circuits which follow. Observing the schematic, note that this buffer amplifier is also an operational amplifier and that it is connected to have a gain-of-one and to be non-inverting. The non-inverting input is at the gate of Q421 and the summing point is at the gate of Q425. Field effect transistors are used in the input stage for minimum loading. Current source Q423 not only supplies current to the input pair, but also to the "battery" circuit (R495, Q420). A ten volt drop is maintained across R495 at all times. Thus, the instantaneous voltage at the bases of emitter followers Q422 and Q424 are always at ten volts relative to the common source potential of Q421-Q425. This ten volt drop is maintained even during the signal fluctuations. In effect, R495 acts as a battery because it is fed from a constant current source and because of the low drive impedance furnished by Q422 and Q424. Because Q422 and Q424 apply the R495 drop voltage to the drains of Q421 and Q425, the drain voltages rise and fall in step with the changes at the common source caused by changes in the instantaneous value of the input signal, and the voltage across Q421 and Q425 remains constant. Q420 acts as a constant current "sink" (or source, it doesn't really matter how one views it) for the "battery" circuit. Transistors Q426, Q427, and Q428 provide additional gain and emitter followers Q429 and Q430 provide a low output impedance.

Note that the Retention signal, which is derived from the output of the Chopper Stabilized Integrator, is applied to the Retention potentiometer. As determined by the setting of the Retention dial, a portion of the Retention Signal is routed through R484 and R481 to the input of the Output Buffer Amplifier. This positive feedback is adjusted to exactly compensate signal loss between aperture openings due to leakage of the Sampling Bridge.

SIGNAL CONTROL BOARD (page VIII-7)

The switching circuits consist of relays K501 and K502, along with their associated components. These relays allow the fast sampler to be bypassed when operating in the normal resolution mode. In this mode, K502 is energized and K501 is de-energized. The signal from the preamplifier output is routed through contacts of K502 directly to the Pre-gate Buffer Amplifier (Q500 through Q505). If the instrument is operating in the high resolution mode, the preamplifier output signal is routed through the "B" contacts of K501 to the fast sampler Input Buffer Amplifier (Sampler Board). The output of the buffer is applied to the sampler and its output in turn is applied to another buffer amplifier, also located on the Sampler Board. From here the signal is routed back to the Signal Control board, through the "A" contacts of K501 to the Pre-Gate Buffer Amplifier. The relays are energized by +24 V, which is routed through contacts of the Aperture Range switch as shown by the circuitry in the lower left-hand corner of the Signal Control Board schematic. The line which carries +24 V in the normal resolution mode is designated "NR ENABLE", and that which carries +24 V in the high resolution mode is designated "HR ENABLE".

Pre-Gate Buffer Amplifier

The Pre-Gate Buffer amplifier is another non-inverting, gain-of-one, operational amplifier. It is interposed between the Signal Switching circuits and the Integrator Amplifier. Considering the circuit in some detail, the non-inverting input is at the base of Q500 with the summing junction being at the base of Q503. These two transistors are connected as an emitter coupled amplifier pair, part of the Q500 through Q503 high gain stage. Complementary emitter followers Q504 and Q505 provide a low output impedance. Diodes CR505, CR506, and CR507 establish proper dc levels and compensate the emitter base drops of Q504 and Q505. The gain is established at one by the feedback from the output through R518 to the summing junction at the base of Q503.

Overload Detector Circuit

Note that the preamplifier output is not only applied to relays K501 and K502, but that it is also applied to the input of the Overload Detector circuit at the base of Q506. This circuit, which comprises Q506 through Q511 and their associated components, monitors the instantaneous signal level at the output of the Preamplifier and powers the front panel Overload light if the signal exceeds a predetermined level.

Current source Q507 furnishes current to the input pair, Q506 and Q508. The collectors of these transistors are applied to diodes CR508 and CR509. Quiescently, both of these diodes are reversed biased and Q509 is cut off. The collector of Q509 is at -1.2 V because of conduction through diodes CR511 and CR512. With Q509 cut off, Q511 is cut off as well and the Overload light does not glow. Note that Q510 conducts quiescently because of the current supplied to its base through R540, and, if the instrument is operating in the high resolution mode, through R543 as well. The R543 circuit is in the circuit only in the high resolution mode, thus establishing a different "threshold" level for the two modes. This shift in overload indication threshold corresponds to the actual difference in overload tolerance exhibited by the instrument in the two modes.

As the signal at the output of the Preamplifier goes positive, current increases through Q506, lowering the voltage at the collector of that transistor. If the voltage drops below the base voltage at the base of Q510, CR509 will be forward biased and Q509 will conduct. When Q509 conducts, Q511 conducts and the Overload Lamp lights. Similarly, if the signal at the output of the Preamplifier goes negative, current increases through Q508 and the collector voltage of that transistor drops. If the preamplifier output goes sufficiently negative, the collector voltage of Q508 drops below the Q510 bias voltage. This time CR508 conducts. Again, Q509 conducts, Q511 conducts, and the Overload light turns on.

Note the network associated with Q511. Its effect is to hold the Overload light in conduction long enough to be noticed with short input overload transients. This effect is achieved as follows. As Q511 is biased into conduction, its collector voltage drops. This drop is rapid because of the low impedance discharge path for C510 through CR511. When the turn-on transient is removed, Q511 starts to turn off and its collector voltage rises. As it rises, CR511 is turned off and CR512 effectively connects the rising collector voltage to the base of Q511 in a sort of "Miller Integrator". As a result of this positive feedback, Q511 remains in conduction for the time required to charge the capacitor. When the capacitor finally charges, Q511 cuts off, and both CR511 and CR512 are forward biased by the current supplied by R537.

Output Buffer (inverting) Amplifier

The Output Buffer Amplifier, Q512 through Q518, is interposed between the output of the Integrator Amplifier and the various instrument outputs. Unlike most of the amplifiers used in the Model 160, this one inverts the applied signal. This inversion compensates the inversion provided by the Integrator Amplifier and assures that the outputs are of the same polarity as the input. This amplifier drives the meter and other outputs as shown on the schematic. The retention signal, simply a fraction of the output voltage as determined by the setting of the Retention control, is also taken from the output of this amplifier.

Referring to the schematic, note that Q512 and Q513 are a conventional emitter coupled amplifier pair. Transistors Q514, Q515, and Q516 constitute a high gain stage, and emitter followers Q517 and Q518 provide a low impedance output. The gain is established by the ratio of R546 to R544 at one.

PREAMPLIFIER BOARD (page VIII-8)

The Preamplifier is a high frequency, non-feedback amplifier with a gain of approximately twenty-0ix. Referring to the schematic, note that the Preamplifier is divided into four sections, a gain-of-one input stage, two amplifier stages (X6.5 and X3.7 respectively) and a gain of one output stage.

Considering the schematic in greater detail, note that the input signal is applied to the Preamplifier at the gate of Q1100A, one half of the dual source follower input stage. Transistors Q1101 and Q1102 act as constant current sources for the source followers. Trim-potentiometer R1120 allows any offset voltage to be compensated. The front panel adjustable, calibrated, offset voltage is applied through R1107 to the gate of Q1100B as well. Trim-potentiometer R1116 is a temperature compensation adjustment for

the input stage. Switch S1100 is one of the two reed switches located on the board. This switch is used in aligning the amplifier as outlined in Section V. From the source followers, the signal is applied to the following gain-of-6.5 stage, Q1103 through Q1107. Q1103 is a current source for the emitter coupled amplifier pair, Q1104-Q1105. These two transistors drive common base stages Q1106 and Q1107, which in turn drive the following amplifier stage. The gain of the X6.5 stage is determined by the ratio of the collector resistors of Q1106 and Q1107 to the net emitter impedance, with R1130, R1128, R1129, C1109, and C1110 all contributing. Trim-capacitor C1109 allows the high frequency gain of the Preamplifier to be properly set.

The following amplifier stage, Q1108 through Q1111, is similar, except that the emitter coupled pair, Q1100 and Q1111, is not fed from a transistorized constant current source. As before, the emitter coupled transistors drive a pair of common base amplifiers, Q1108-Q1109, and the gain (X3.7) is a function of the collector resistors and the net emitter impedance.

The final stage, Q1114 through Q1117, consists of four transistors connected as two complementary emitter followers. Diodes CR1104 and CR1105 compensate the emitter base drops of Q1114 and Q1116, while diode diodes CR1106 and CR1107 compensate the emitter base drops of Q1115 and Q1117.

Differential pair Q1112-Q1113 constitutes the heart of a common mode feedback loop which assures that the two outputs will really be the complement of one another. The two outputs are summed at the base of Q1112 after being routed through resistors Q1154 and R1155. Note that the base of Q1113 is returned to ground and that Q1112 feeds back to Q1103 to control the current supplied by Q1103. If the sum of the two outputs is not zero, the feedback adjusts the current supplied by Q1103 as required to bring the output back into balance.

CHOPPER STABILIZED INTEGRATOR (page VIII-9)

As discussed elsewhere, the function of the chopper stabilized integrator is to accurately average a signal during the selected aperture time and then to store that average value over the interval between successive aperture openings. The integrator's ability to store the average value between aperture openings is expressed in the holding time specification, which is one of the prime performance specifications of the instrument. The integrator's ability to achieve a long holding time depends on the leakage of the feedback capacitor and on the input offset current at the summing junction of the amplifier. Assuming a "perfect" capacitor (one having negligible leakage current relative to the input offset current of the amplifier), the change in amplifier output voltage with time is given by:

$$\frac{dV}{dt} = \frac{i_{in}}{C_{fb}} ,$$

where $\frac{dV}{dt}$ is the memory drift at the output in volts per second, i_{in} is the input current to the summing junction in amperes, and C_{fb} is the capacitance of the feedback capacitor in farads. Because the input current, i_{in}, is typ-

ically in the range of ±5 pA and the minimum capacitance is 1 nF (C701), the maximum typical drift rate is ±5 mV/s. This drift is determined almost solely by the offset current; the leakage current of the 1 nF feedback capacitor is much less than the 5 pA of offset current. When longer time constants are switched in, the size of the feedback capacitor is increased, improving the drift rate as shown in Table III-3 on page III-28. However, these larger capacitors have higher leakage currents as well, and with time constants of 3 ms or larger, the capacitive current predominates and limits the improvement in memory drift to about 100 μV/s, the typical memory drift for time constants of 3 ms or longer.

Referring to Figure IV-12, a block diagram of the Chopper Stabilized Integrator, note that the amplifier is divided into two sections, a low frequency section (Modulator-Amplifier-Demodulator) and a high frequency section (Q701-Q707). Ideally, the voltage at the summing junction of a high-gain operational amplifier should be exactly zero. The low frequency amplifier section is instrumental in approaching this ideal. First, it senses any error or non-zero voltage at the summing junction. Then the modulator section, which comprises phototransistors R745 through R748, "chops" the error signal with respect to sense ground at a frequency of 77 Hz (nominal). The resulting ac signal is then summed with any high frequency signals passed through C702 and further amplified by Q701 through Q707. The output is applied through the feedback element to the summing junction to drive it to zero relative to sense ground. In this way, not only is the error signal at the summing point servoed to an acceptable level, but the low frequency (including dc) gain is multiplied to a very high level (approximately 100 million) because both amplifier sections are effectively cascaded. Figure IV-13 shows the typical open loop gain versus frequency characteristic for the amplifier without a feedback capacitor.

The requirement for extremely low offset voltage and high open-loop gain is dictated by the need for negligible input current. The input current is a function of the offset voltage and the resistance from the summing junction to ground (approximately two megohms). Two factors, modulator defects and finite amplifier gain, determine the offset voltage. Potentiometer R1001 corrects for small fixed offsets at the summing junction as well as for any lack of perfect matching between transistors Q701 and Q702.

The Modulator-Demodulator is controlled by a free-running relaxation oscillator consisting of neon bulbs DS1 and DS2, resistors R726 and R727, and capacitor C707. When DS1 is conducting (in a "glow" state), DS2 is non-conducting and "dark". This phase relationship is maintained in modulator photoresistors R746 and R747, and in demodulator photoresistors R741 and R742 by causing the conductance of these photoresistors to increase while their symmetrical counterparts, R745 and R748 (modulator), and R740 and R743 (demodulator) are in a low conductance state. As the oscillator switches state at the 77 Hz rate, so does the conductance of the photoresistors. The modulator converts any dc at its input to a 77 Hz ac signal. The demodulator "reconstructs" the amplified ac signal into a dc level proportional to the input dc.

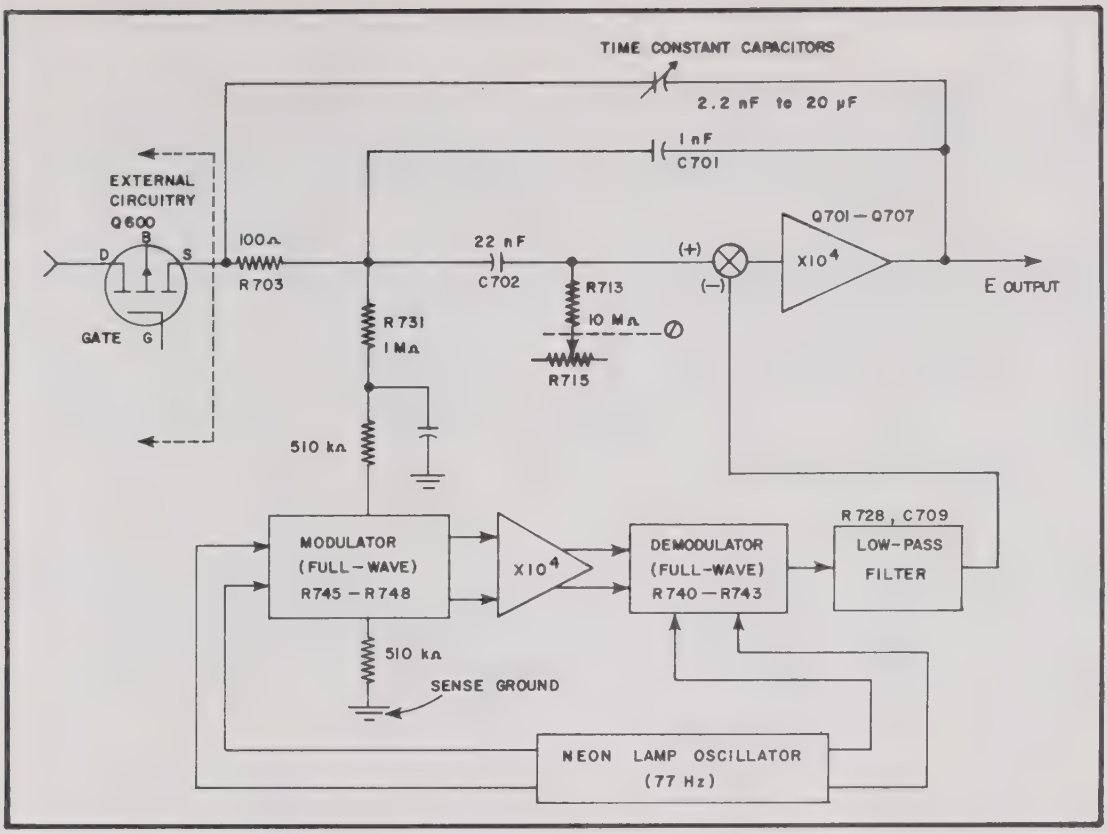


Figure IV-12. BLOCK DIAGRAM OF CHOPPER STABILIZED INTEGRATOR

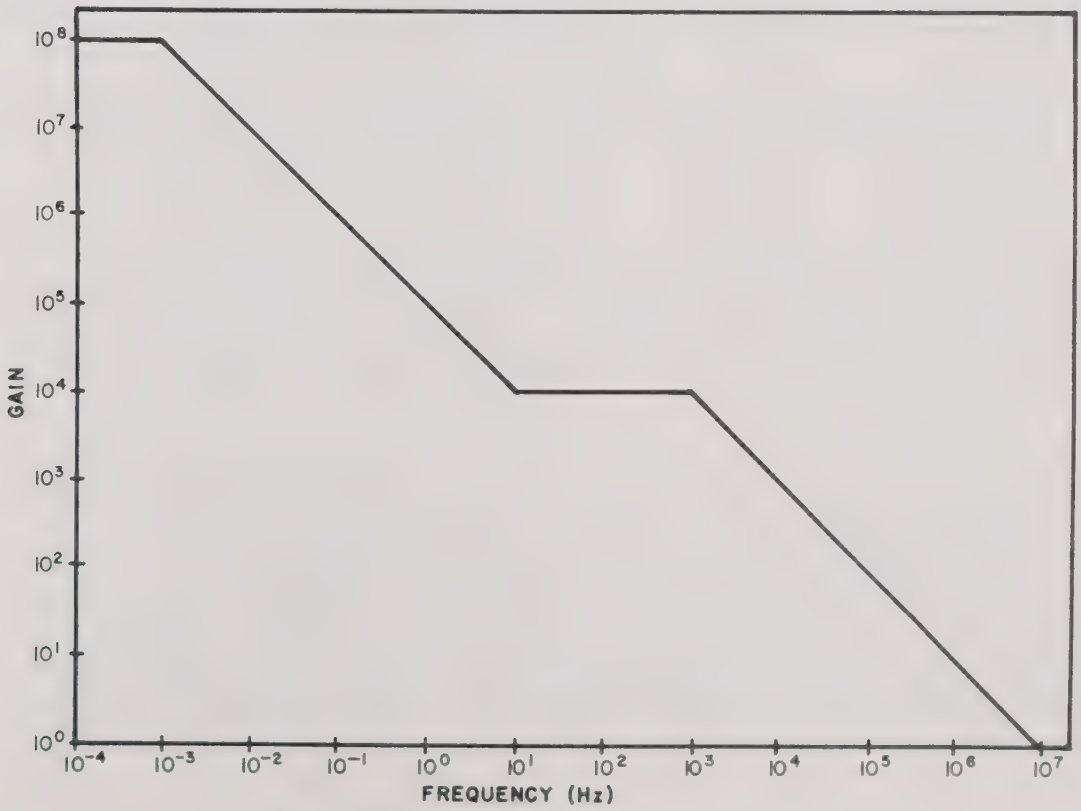


Figure IV-13. GAIN VERSUS FREQUENCY RESPONSE

POWER SUPPLY BOARD (page VIII-10)

The reference, sensing, and regulation circuitry for the five regulated power supplies (±24 V, ±12 V, and +4.5 V) are contained on a single circuit board. With the exception of the +4.5 V supply, the power output stages (series pass transistors) are physically located on the Chassis mounted heat sink. Because the 4.5 V supply operates at low power levels, its pass transistor does not develop excessive heat, and so is mounted on the circuit board.

The +24 V supply serves as the master reference source for all of the other supplies. Because of this, and because it is similar to the other supplies (with the exception of the +4.5 V supply), the following circuit description will concentrate mainly on the +24 V supply.

Referring to Figure IV-14, a block diagram of the +24 V supply, note that this supply may be regarded as a classic operational amplifier with a power booster as an output stage. In the case of the +24 V regulator, the feedback circuit is that of a non-inverting amplifier whose output is a function of the reference voltage (Zener diode CR1000) and of the feedback network. Overload protection is provided. If the current approaches 600 mA, Q1002 causes the collector voltage of Q1001 to drop towards zero, thus protecting the output transistor (Q1) from overload-induced damage.

Assuming the supply is regulating, zener diode CR1000 supplies a stable 9 V (nominal) reference voltage to the non-inverting input of A1001. A fraction of the output voltage, as determined by R1000, R1001, and R1002, is fed back to the inverting input of the operational amplifier. Potentiometer R1001 is adjusted to establish the output voltage at +24 V; the adjustment allows for normal tolerance variations in zener diode CR1000. Transistor Q1003 provides additional amplification. Note from the schematic (page VIII-10) that the

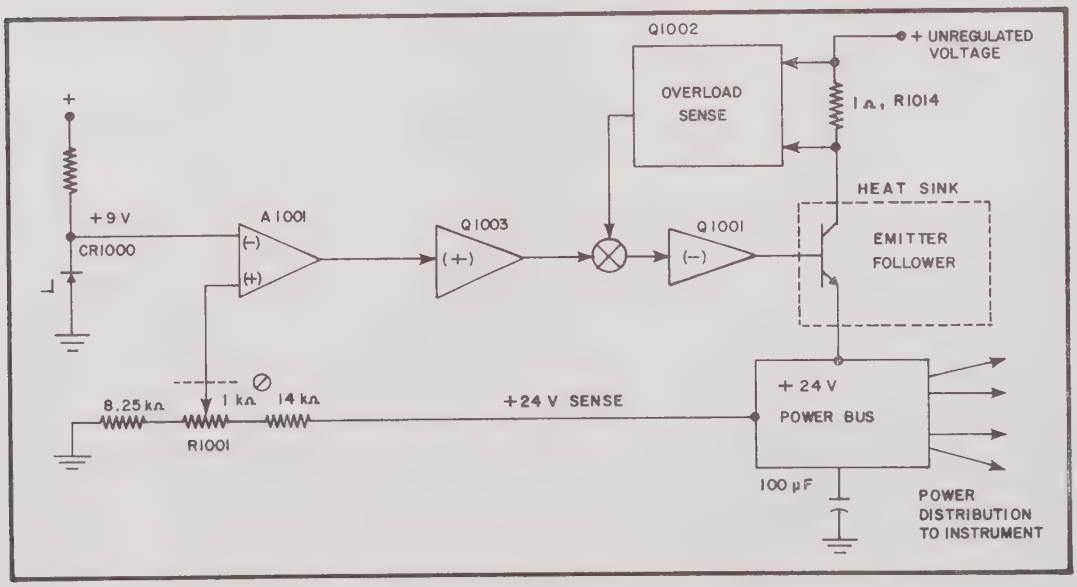


Figure IV-14. BLOCK DIAGRAM OF +24 V POWER SUPPLY

base of Q1003 is held at a voltage of approximately +9 V. When the instrument is first turned on, however, R1010 and R1011 provide a temporary base bias of +7 V through diode CR1003 to bring the loop into equilibrium quickly. As soon as the supply begins regulating, this "start-up" bias circuit is effectively disconnected because CR1003 becomes reverse biased.

Transistor Q1001 provides additional drive to the output emitter follower, Q1. It also acts to lower the output voltage to zero should a short circuit occur. This is accomplished in the following manner. As the current through the pass transistor increases, so does the voltage drop across resistor R1014. Should the current approach 600 mA, the emitter-base junction of Q1002 becomes forward biased, causing the collector voltage of Q1002 to rise toward the level of the unregulated voltage. When this happens, Q1001 is biased off, causing its collector voltage, and hence the emitter voltage of Q1, to drop to zero, thereby limiting any short circuit current to 600 mA.

Three of the other regulated supplies, -24 V, +12 V, and -12 V, function in an almost identical manner, the only differences being in the actual output levels and in that some are connected in an "inverting" and some in a "non-inverting" configuration. Note that the +24 V supply output serves as the reference for the -24 V supply and for the +12 V supply. The -24 V supply, in turn, is used as the reference for the -12 V supply and for the +4.5 V supply. Because the +24 V supply acts as the "master" reference, it must be functioning properly for any of the other supply levels to be normal.

The +4.5 V regulator differs from the others in two respects; it does not incorporate an integrated circuit amplifier and it does not have an external (to the circuit board) power output stage. A simple two-transistor differential stage is employed, with the base of Q1016 serving as the inverting input (summing junction) and the base of Q1015 serving as the non-inverting input. The non-inverting input is returned to ground through R1058. Because of the feedback through R1063, the output is regulated to the level required to maintain zero volts at the base of Q1016. Moreover, because the summing junction is also returned to -24 V through R1062, the output level will be +4.5 V, as determined by the feedback and the R1063-R1062 voltage divider.

The three diodes in series, CR1025, CR1026, and CR1027, act as a current limiter. Normally these diodes are reverse biased. However, when the current approaches two amperes, the drop across resistor R1061 becomes large enough to bias the diodes into conduction. As the diodes conduct, they shunt the drive to the base of Q1014, causing a drop in output voltage and limiting the current to a maximum of about two amperes.

ANALOG STORAGE ACCESSORY BOARD (page VIII-15)

Memory Enable Logic Circuit

This circuit senses the position of the front-panel Trigger Mode and Memory switches. As explained in subsection 4.6 (ANALOG STORAGE MODULE), the output of this circuit "enables" the integrated circuit monostable. Observing the schematic, note that, if the Trigger Mode switch is set to EXT. and the Memory switch is set to ON, Q801 conducts to supply current to K801, the relay which allows the analog storage circuit to be connected to the summing

point of the chopper stabilized integrator, and to the front-panel Memory light. If the switches are not in the indicated positions, Q801 does not conduct, the Memory light does not turn on, and K801 is not energized, thereby isolating the analog memory circuit.

Emitter follower Q802 also senses the +4.5 V applied from the switch contacts and supplies this voltage to the monostable, allowing it to become active. If the switches are not in the indicated position, the emitter of Q802 will be near ground and the monostable will be disabled as explained in subsection 4.6.

Gate Buffer

This circuit is simply an emitter follower, Q803, which buffers the gate pulse prior to applying it to the monostable input. Note that there are two inputs, one for internally derived pulses (AT line through R808) and one for externally derived gate pulses. Pulses of external origin are routed through the diode/resistor shaping network (R803 and following components) prior to application to the base of Q803.

Monostable

Subsection 4.6 contains a detailed description and truth table for the operation of this circuit.

Switch Driver

The switch driver, Q806 and Q807, accepts the 5 ms pulse generated by the monostable and provides the complementary pulses appropriate for controlling the two field effect transistors, Q804 and Q805.

Storage and Shaping

See subsection 4.6 for a detailed description of how the storage capacitor, C806, is switched to achieve the memory function.

SECTION V
ALIGNMENT PROCEDURE

5.1 INTRODUCTION

The Model 160 Boxcar Integrator is a conservatively designed reliable instrument and as such, should provide long dependable service. However, as an assurance of maintaining the highest confidence in experimental measurements, the following alignment procedure should be performed after one year and at one year intervals thereafter.

The procedure should be performed in its entirety and in the order indicated. An occasion may arise, such as after a repair, where it may suffice to align a single circuit or group of circuits. However, a decision to make a partial alignment should be reserved to someone having sufficient knowledge of the circuitry to fully understand all possible interactions.

Should any problems arise in the course of making the alignment, contact the factory or a factory authorized representative, a list of whom appears at the end of the manual.

5.2 EQUIPMENT NEEDED

(1) 23 pin extender board, PAR # EB1337.

(2) 35 pin extender board, PAR # EB2573.

(3) Fast risetime, general purpose pulse generator.

Suggested Instrument --- TEKTRONIX type 114.

(4) Wideband general purpose oscilloscope with dual trace capabilities.

Suggested Instrument --- TEKTRONIX type 454 or type 544 with a type 1A2 plug in.

(5) Four place digital voltmeter.

Suggested Instrument --- NLS type X2.

(6) Power Supply 0-to-15 V, 1% accurate.

(7) Counter capable of measuring a period of 20 μs with an accuracy of ±0.2 μs or better. If the oscilloscope time base is accurate enough to make the measurement, or if a sufficiently accurate source of marker pulses is available, the counter will not be required.

Suggested Instrument --- HP5325A

(8) Center zero dc voltmeter.

Suggested Instrument --- HP419A.

(9) Multimeter such as the Simpson 260.

(10) Small bar magnet for activating reed switches.

5.3 GENERAL TECHNIQUE

(1) Never remove or replace a circuit board with the power on. Otherwise sensitive components will almost certainly be damaged.

(2) When measuring voltages, use a ground reference as close as possible to the point being monitored. If the board has a "ground plane", use the ground plane as the reference.

(3) When making high frequency oscilloscope measurements, keep the ground path between the probe and the ground plane as short as possible. To minimize the inductance of this path, it is suggested that a short length of shielding braid be used.

(4) When measuring the voltage at a high-impedance or sensitive point, such as the summing junction of an amplifier, connect a resistor (typical value somewhere in the range of 1 kΩ to 5 kΩ) between the voltmeter and the monitored point to reduce the capacitance between the circuit and the voltmeter, thereby reducing the likelihood of oscillations or degraded circuit performance. Physically, the resistor should be located at the monitored point and not at the voltmeter.

(5) Note that a tolerance is given for each adjustment in the procedure. If, upon measuring, it is found that the parameter in question is within tolerance, do not change the setting of the controlling adjustment.

5.4 PRELIMINARY STEPS

(1) Remove the top and bottom covers of the instrument. Then remove the decorative strip from the bottom. This decorative strip is between the front panel and the bottom cover. Finally, remove the board locking bar, which is secured by two screws (1/4 x 6-32).

(2) Remove the Power Supply Board (Figure V-1 on page V-4 shows the location of the boards, adjustments, and test points). Then mount the Power Supply Board in the 23 pin Extender Board and return the "combination" to the Power Supply Board socket.

(3) Turn on the power and allow the instrument to warm up for five minutes.

5.5 POWER SUPPLY LEVELS

(1) Check the following unregulated supply levels at the indicated pins of the Power Supply Board. These levels apply with a line voltage of 117 Vac.

Pin	Voltage	Tolerance (±)
1	+10 V	2 V
13	+32 V	3 V
7	-32 V	3 V
16	+18 V	2 V
22	-18 V	2 V

(2) Monitor the voltage at the red test point with the DVM (digital voltmeter). The voltage should be +24.00 V. If it is not within tolerance, adjust R1001 (+24 V ADJ.) for an indicated voltage of +24.00 V. Then proceed to check the regulated supply levels at the other test points as follows.

Test Point	Voltage	Tolerance (±)
yellow	-24.0 V	0.04 V
blue	+12.00 V	0.04 V
white	-12.00 V	0.04 V

(3) Monitor the voltage at pin 3. The indicated voltage should be +4.5 V ±0.1 V.*

(4) Use the oscilloscope to check the ripple and noise at each of the power supply test points and at pin 3. In each case the combined ripple and noise should be less than 40 mV pk-pk.

(5) Turn off the power. Then remove the extender board and return the Power Supply Board to its socket.

5.6 PREAMPLIFIER

(1) Remove the Preamplifier Board from its socket. Then mount it in the extender board and return the "combination" to the Preamplifier Board socket.

(2) Turn on the power and allow a five minute warmup period.

(3) Set the front panel controls as follows.

Trigger Mode	EXTERNAL
Prefilter	OFF
Coupling	GND
Sensitivity	50 mV
Input Selector	50Ω
Input Offset	OFF
Aperture Time Range	"blue"

(4) Note the two reed switches (narrow glass capsules) mounted on the Preamplifier Board. These switches serve as jumpers where use of clip

*In the case of units having serial numbers of 140 or higher, the voltage is +4.75 V ±0.2 V.

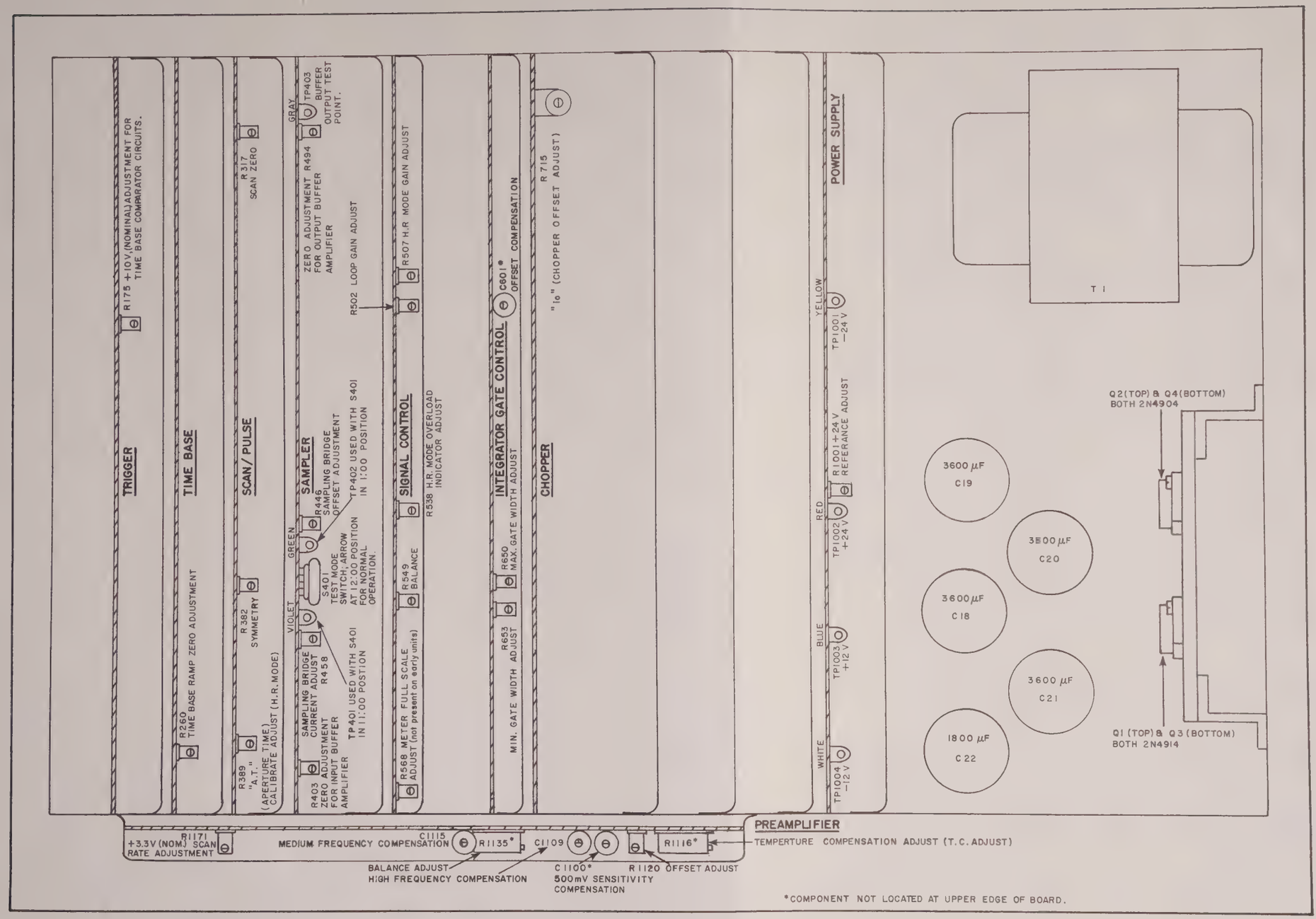

TRIGGER
R175 +10V (NOMINAL) ADJUSTMENT FOR TIME BASE COMPARATOR CIRCUITS.
TIME BASE
R260 TIME BASE RAMP ZERO ADJUSTMENT
SCAN/PULSE
R389 "A.T." (APERTURE TIME) CALIBRATE ADJUST (H.R. MODE)
R382 SYMMETRY
R317 SCAN ZERO
SAMPLER
R403 ZERO ADJUSTMENT FOR INPUT BUFFER AMPLIFIER
SAMPLING BRIDGE CURRENT ADJUST R458
TP401 USED WITH S401 IN 1:00 POSITION
S401 TEST MODE SWITCH; ARROW AT 12:00 POSITION FOR NORMAL OPERATION.
TP402 USED WITH S401 IN 1:00 POSITION
R445 SAMPLING BRIDGE OFFSET ADJUSTMENT
R502 LOOP GAIN ADJUST
ZERO ADJUSTMENT R494 FOR OUTPUT BUFFER AMPLIFIER
TP403 BUFFER OUTPUT TEST POINT.
SIGNAL CONTROL
R568 METER FULL SCALE ADJUST (not present on early units)
R549 BALANCE
R538 H.R. MODE OVERLOAD INDICATOR ADJUST
R507 H.R MODE GAIN ADJUST
INTEGRATOR GATE CONTROL
R653 MIN. GATE WIDTH ADJUST
R650 MAX. GATE WIDTH ADJUST
C601* OFFSET COMPENSATION
CHOPPER
R715 "Io" (CHOPPER OFFSET ADJUST)
POWER SUPPLY
TP1001 −24 V
R1001 +24 V REFERANCE ADJUST
TP1002 +24 V
TP1003 +12 V
TP1004 −12 V
T1
Q2(TOP) & Q4(BOTTOM) BOTH 2N4904
Q1 (TOP) & Q3 (BOTTOM) BOTH 2N4914
3600 μF C19
3600 μF C20
3600 μF C18
3600 μF C21
1800 μF C22
PREAMPLIFIER
R1171 +3.3V (NOM.) SCAN RATE ADJUSTMENT
C1115 MEDIUM FREQUENCY COMPENSATION
R1135*
C1109
R1116*
TEMPERTURE COMPENSATION ADJUST (T.C. ADJUST)
BALANCE ADJUST HIGH FREQUENCY COMPENSATION
C1100* 500mV SENSITIVITY COMPENSATION
R1120 OFFSET ADJUST
*COMPONENT NOT LOCATED AT UPPER EDGE OF BOARD.

Figure V-1. LOCATION OF ADJUSTMENTS AND TESTPOINTS

leads might cause the circuit to oscillate. They are activated by holding one pole of the bar magnet to either end of the reed switch. The parts location diagram located next to the Preamplifier Board Schematic (page VIII-8) identifies these switches.

Monitor pin 14 of the Preamplifier Board with the oscilloscope (use a low-capacitance probe). Then activate reed switch S1101 and ascertain that there are no UHF oscillations at pin 14. Finally, use the voltmeter to monitor the dc voltage at pin 14. Take care to use an isolation resistor as described under GENERAL TECHNIQUE. The measured voltage is typically a few hundred millivolts. Record the measured voltage.

(5) Deactivate reed switch S1101 and activate S1100 instead. Then adjust R1135 (BALANCE) so that the voltage at pin 14 is the same (±5 mV) as was obtained in step 4. Continue checking with the oscilloscope to ascertain that the circuit is not oscillating (if the circuit is oscillating, the measurements may be invalid). After completing the adjustment, deactivate S1100.

(6) Set R1120 (OFFSET) to the center of its range. Then ground the wiper of this trim-potentiometer with a short clip lead and, after so doing, adjust R1116 (TEMPERATURE COEFFICIENT) so that the voltage at pin 14 is again the same (±5 mV) as was recorded in step 4.

(7) Remove the clip lead and readjust R1120 (OFFSET) for 0 mV ±1 mV at pin 14.

(8) Set the Input Coupling switch to AC. Then note and record the voltage at pin 14. After so doing, rotate the Sensitivity switch through all its positions, measuring the voltage at pin 14 in each position. In each position the voltage should be within two millivolts of the recorded voltage.

(9) Measure the voltage at pin 23 of the Preamplifier Board. The indicated voltage should be +45 mV ±100 μV. This voltage should be measured relative to the Preamplifier ground, pin 16.

(10) Set the Sensitivity switch to CAL. and measure the voltage at pin 14 using the digital voltmeter. Continue using the isolation resistor in making these measurements. The measured voltage should fall in the range of +0.90 V to +1.1 V. Record the measured voltage.

(11) Transfer the voltmeter (and the isolation resistor) to pin 19. Record the indicated voltage which should be negative. The magnitude of this voltage should be within one percent of the average of the magnitude of this voltage and that recorded in step 10.

(12) Transfer the voltmeter (and the isolation resistor) back to pin 14. Then set the Sensitivity switch to 10 V and turn the Offset dial (front panel) fully clockwise. Set the Offset Polarity switch to "+" and the Offset Scale switch to "X1". The voltage at pin 14 should be the same (±20 mV) as that recorded in step 10.

Set the Offset Scale switch to "X10". The indicated voltage should increase a factor of ten (±200 mV).

(13) Monitor pin 14 with the oscilloscope (leave the voltmeter attached as well). Then set the Sensitivity switch to 1 V and the Coupling switch to AC. The Offset Scale switch should be set to X10 and the Offset Polarity switch to "+". Note the indicated dc level.

(14) Adjust the controls of the pulse generator for a 2 V pk-pk square wave at 10 kHz. Then connect this signal to the 100 kΩ input of the Model 160. The signal at pin 14 should be an undistorted replica of the input signal. With the input signal applied, the dc level at pin 14 should shift no more than 100 mV.

Set the Offset Polarity switch to OFF. The dc level at pin 14 should drop to zero but the signal should remain unchanged.

Set the Offset Polarity switch to "-". The dc level at pin 14 should be negative, but its magnitude should be the same (±200 mV) of what it was with the Offset Polarity switch set to "+". The signal should remain unchanged. Leave the Offset Polarity switch in the OFF position.

(15) Adjust the controls of the pulse generator to produce a 1 MHz square wave. Use 50Ω attenuators (General Radio type preferred) to obtain 100 mV pk-pk when the output is terminated in 50Ω. Then remove the termination and connect the signal to the 50Ω input of the Model 160.

(16) Make provision for monitoring the signal at the violet test point on the Sampler board. Be sure that the oscilloscope probe is properly compensated for both low and high frequency response.

(17) Turn off the power. Then separate the Preamplifier Board from the extender, remove the extender, and return the Preamplifier Board to its socket. Turn the power back on.

(18) Set the Sensitivity switch to "50 mV" and note the displayed signal. It should be a 1 MHz square wave with a peak-to-peak amplitude of approximately 2 V (±200 mV with 10:1 attenuator probe).

Adjust trim-capacitor C1109 for the fastest rise time in the observed square wave. Typically, this will be on the order of seven nanoseconds. However, the rise time obtained will depend on the rise time of the pulse generator and oscilloscope as well; the observed rise time will equal the square root of the sum of the squares of the individual rise times, rise time defined as the 10% to 90% transition time.

Adjust trim-capacitor C1115 for an approximately two percent overshoot* on the observed waveform. Figure V-2 shows the input square wave and

*For a certain class of applications it may be desirable to have other values of overshoot. The exact amount of transient compensation is then a prerogative of the experimenter and should be adjusted accordingly.

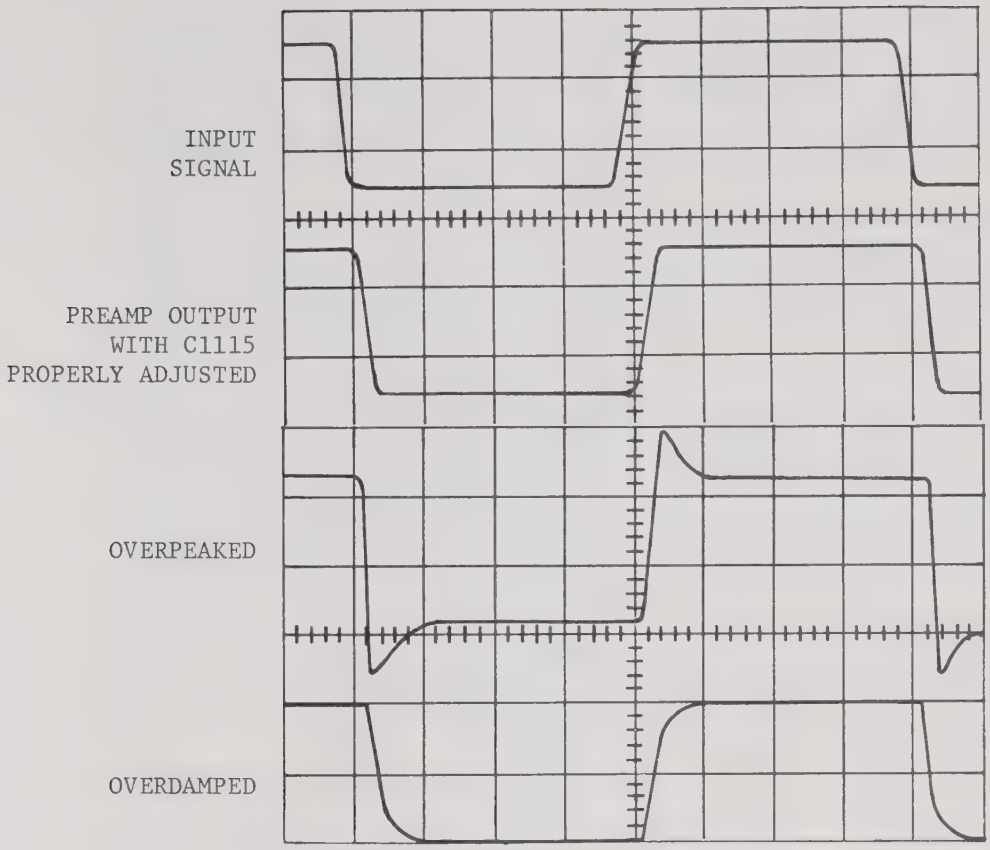


Figure V-2. EFFECTS OF ADJUSTING CAPACITOR C1115

the signal at the Preamplifier Output jack when C1115 is correctly set, and incorrectly set. It should be mentioned that it is essential that the Preamplifier Board not be on an extender when these capacitors are adjusted.

(19) Set the Sensitivity switch to "10 V" and increase the amplitude of the input square wave to 10 V pk-pk. Reduce the frequency of this signal to 10 kHz. While continuing to monitor the Preamplifier Output jack (the observed signal should have an amplitude of approximately 1 V pk-pk), adjust C1220 for the best square wave response. This trim capacitor as well as trim capacitor C1231 are located on the Sensitivity switch as shown in Figure V-3.

(20) Check the square wave response on the 5 V, 2 V, and 1 V positions of the Sensitivity switch, using a full scale input signal in each case. If one of these positions shows a poor square wave response, it is a sign that one of the components associated with that position of the switch has changed value or been damaged.

(21) Reduce the amplitude of the input square wave to 1 V pk-pk and set the

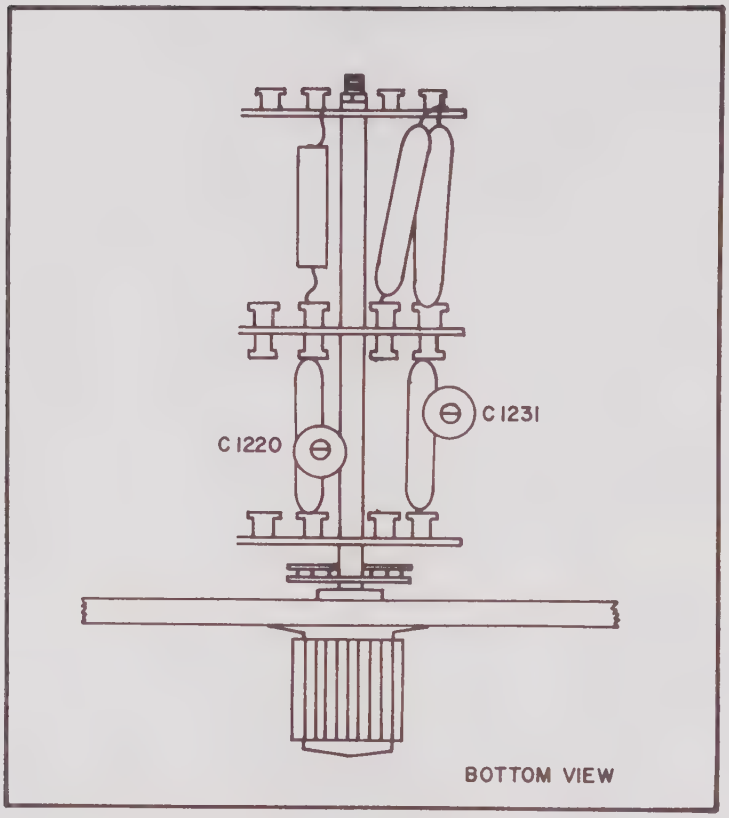


Figure V-3. LOCATIONS OF CAPACITORS C1220 AND C1231

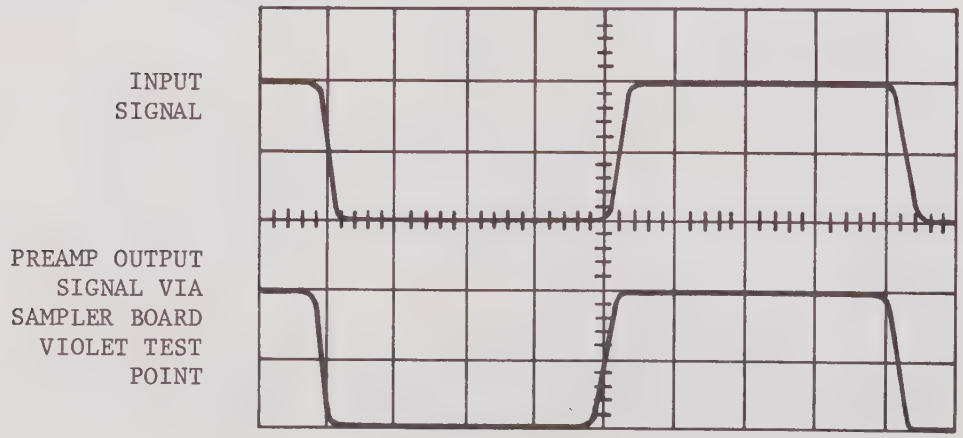


Figure V-4. TYPICAL SQUARE WAVE RESPONSES WHEN ADJUSTING CAPACITORS C1220, C1100, AND C1231

Sensitivity switch to 500 mV. Then adjust C1100, located on the Preamplifier Board, for the best square wave response.

(22) Further reduce the input signal to 0.5 V pk-pk and set the Sensitivity switch to 200 mV. This time adjust C1231 for the best square wave response.

(23) Check the Square wave response on the 100 mV and 50 mV sensitivities, using a full scale input signal in each case. If one of these positions shows a poor square wave response, it is a sign that one of the components associated with that position of the switch has changed value or been damaged.

(24) Set the sensitivity to "500 mV" and adjust the input signal amplitude to 1 V pk-pk. Then begin rotating the Prefilter switch counterclockwise, noting that the rise time of the preamplifier output signal increases as the switch is rotated, and that the rise time in each position is approximately that given by the Prefilter switch symbolization. In the "1 MHZ" position, the rise time should be 150 ns ±30 ns. In the other positions, the rise time should be verified merely by "ball park" estimates.

5.7 TRIGGER BOARD - Test Procedures are for reference only. No adjustments are performed in the Trigger Board test procedure sequence.

(1) Set the Model 160 Controls as follows.

Trigger Mode	EXT.
Time Base Mode	INT.
Slope	+
Threshold	2 o'clock (slightly clockwise relative to "0")
Time Base Duration	20 µSEC.
Trigger Delay	50%
Trigger Delay Mode*	DIAL
Initial Delay	5%
Final Delay	100%
Scan Mode	DELAY
Stretch Time	10 µSEC.
Aperture Time	1 µSEC. (normal resolution mode)

(2) Adjust the pulse generator controls to provide a +3 V, 100 ns wide output pulse with a repetition period of 1 µs. Then connect this output to the Trigger Input of the Model 160.

(3) Trigger the oscilloscope coincident with the leading edge of the pulse generator output. Many pulse generators provide a separate trigger output which can be used for this purpose.

*This switch not provided in early units.

(4) Monitor pin 17 of the Trigger Board with the oscilloscope. It is better to measure the signal without using an extender board. A convenient way to do this is to reset the instrument on its side with the bottom cover removed. One can then easily monitor any pin of any board. The observed signal should be a positive two volt pulse with a duration of ten to thirty nanoseconds as shown in Figure V-5.

(5) Set the Model 160 Slope switch to "-" and observe that the pulse at pin 17 shifts approximately 100 ns later in time.

(6) Increase the amplitude of the pulse generator output until the ampli-

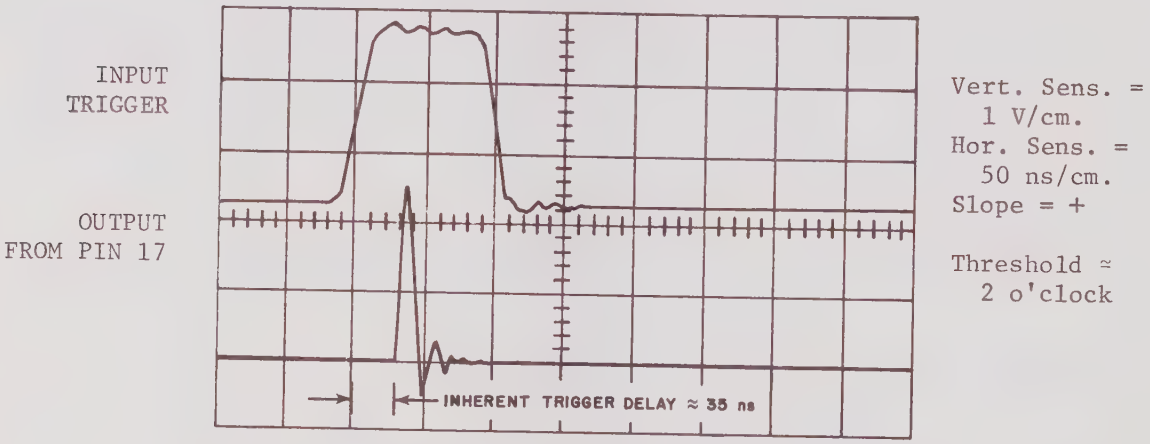


Figure V-5. INPUT TRIGGER AND TRIGGER BOARD OUTPUT

tude of the signal applied to the Model 160 input is +5 V (including overshoot). Then, while continuing to monitor the signal at pin 17, begin turning the Threshold control clockwise. Just before the control reaches the fully clockwise position, the pulse at pin 17 should disappear. Leave the Threshold control in the fully clockwise position.

(7) Reverse the polarity of the pulse generator output. Check that the amplitude of the pulse generator output is exactly -5 V. If necessary, adjust the pulse to that level. Then reconnect the oscilloscope to pin 17.

(8) Begin turning the Threshold control counterclockwise. Initially there will be no signal at pin 17. However, as the Threshold control crosses "0", the Model 160 will begin triggering as evidenced by the reappearance of the pulse at pin 17. Continue turning the Threshold control counterclockwise. Just before the control reaches the fully counterclockwise position, the pulse at pin 17 will disappear again. Leave the Threshold control set midway between fully counterclockwise and "0" (the pin 17 pulse will reappear).

(9) Reduce the repetition rate of the trigger input to 10 kHz.

(10) Transfer the oscilloscope to the Time Base Output jack (rear panel). The observed signal should be a succession of positive 0-to-10 V linear ramps.

(11) Transfer the oscilloscope to the front-panel Delayed Out jack, which should be terminated in 50 ohms. The observed signal should be a 0-to-1.2 V positive pedestal. Figure V-6 shows how this pedestal appears relative to the ramps at the Time Base Output with a Trigger Delay setting of 30% and a Final Delay setting of 87%. The leading edge of the pedestal can be varied, relative to the beginning of the time base ramp, from 0% to 100% of the time base by adjusting the

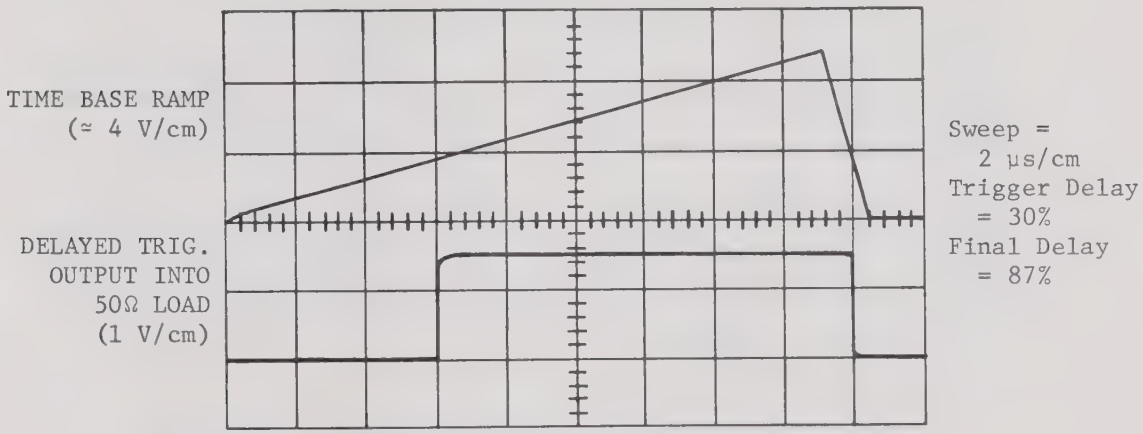


Figure V-6. TIME BASE RAMP AND TRIGGER OUTPUT PEDESTAL

Output Trigger Delay dial. Of course, in order for the trigger delay to reach 100% of the selected time base duration, the Final Delay dial must be set to 100% as well. The pedestal rise time should be 25 ns or less. Leave the Output Trigger Delay dial set to 100%.

(12) Adjust the Final Delay dial to 50%. The pedestal will disappear.

(13) Begin rotating the Output Trigger Delay dial counterclockwise. As the dial approaches 50%, begin turning it slowly while noting the oscilloscope display (the oscilloscope should still be monitoring the Delayed Out jack). The pedestal should reappear when the Output Trigger Delay dial is in the range of 48% to 52%. Leave the Output Trigger Delay dial fully counterclockwise.

(14) Set the Time Base Mode switch to EXT. Then connect the digital voltmeter to the rear-panel Time Base Output jack. The indicated voltage should be 0 V ±0.1 V.

(15) Connect a jumper from pin 6 to the rear-panel Time Base Output jack. The indicated voltage should be +10 V ±0.2 V. Remove the jumper.

5.8 TIME BASE BOARD

(1) Set the Model 160 controls as follows.

Initial Delay	0%
Final Delay	100%
Time Base Mode	INT.

(2) Turn off the power. Then remove the Time Base Board, mount it on an extender board, and return the combination to the Time Base Board socket. Turn the power back on.

(3) Using the dual trace oscilloscope, monitor pin 19 with channel one and pin 7 with channel two. The oscilloscope should be triggered coincident with the negative going edge of the pin 19 signal. (The Model 160 should still be triggered from the 10 kHz pulse generator output.) A convenient sweep time would be 100 ns/cm.

Figure V-7 shows the two signals. Adjust R260, if required, such that the leading edge of the pin 7 signal begins approximately 100 ns later than the leading edge of the pin 19 signal. Then begin dialing the Initial Delay dial clockwise. The leading edge of the pin 7 signal should occur later in time as the dial is turned. There should be no jitter or uncertainty (such instability is most likely to occur in the first few percent of advancement). Should any jitter be noted, turn R260 further clockwise until the jitter disappears. Then adjust R260 an additional half turn clockwise and go on to the next step.

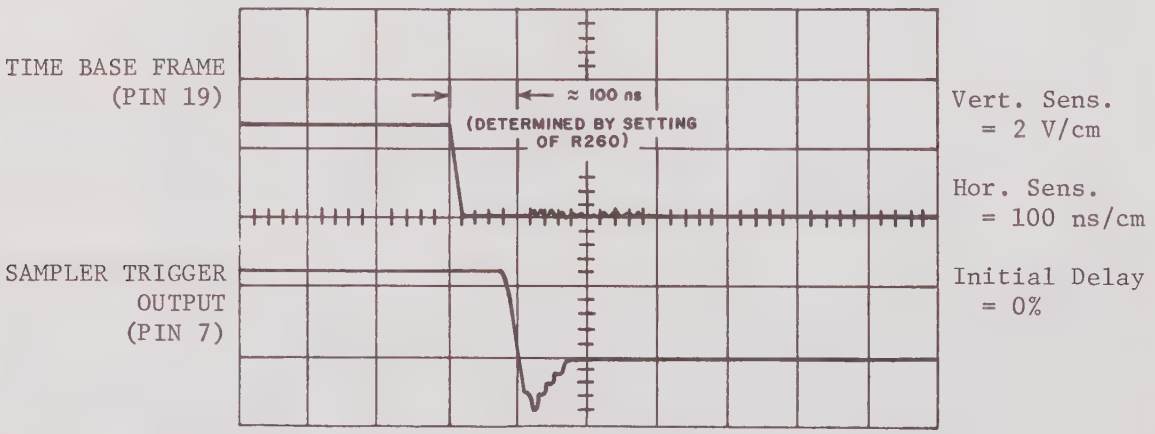


Figure V-7. TIME BASE BOARD SIGNALS AT PINS 7 AND 19

(4) Set the Initial Delay dial to 90%. Then set the Time Base duration to 1 ms and select an oscilloscope sweep time of 100 µs/cm. Carefully note the location of the pin 7 pedestal on the oscilloscope trace. Then begin rotating the Final Delay dial counterclockwise. The pin 7 signal will become increasingly narrow as the Final Delay

dial is turned. Stop with a Final Delay dial setting of 90%. Finally, adjust R176 (located on the Trigger Board) such that the pin 7 signal is a negative "spike" coincident with the trailing edge of the pin 19 signal as shown in Figure V-8.

If R176 is turned too far in one direction, the "spike" will disappear. If turned too far the other way, it will widen into a negative pedestal. Leave the Initial Delay dial set to 0% and the Final Delay dial to 90%.

(5) This step calibrates the time base on the 20 μs time base duration range. The calibration is made by making the interval between the negative transition of the pin 19 signal and the negative transition of the pin

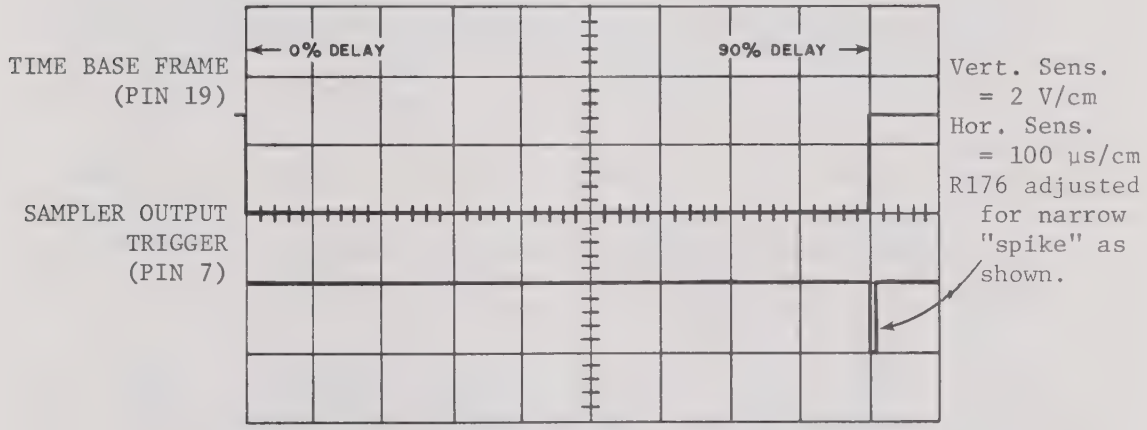


Figure V-8. SIGNALS RELEVANT TO ADJUSTING R176

7 signal 20 μs ±0.2 μs. However, because the adjustment is made with the Final Delay dial set to 90%, the interval is actually set to 90% of 20 μs, i.e., 18 μs ±0.18 μs. Most oscilloscopes do not have a sufficiently accurate time base to make this adjustment. It is possible, however, that a recently calibrated oscilloscope may be sufficiently accurate. Another possibility is to simultaneously provide accurate marker pulses to the oscilloscope. A third is to make the measurement using a period counter having a clock frequency of 5 MHz or higher. The counter should be started by the negative transition of the pin 19 signal and stopped by the negative transition of the pin 7 Signal. If none of these methods are available, it is probably better not to try to calibrate the time base duration.

Assuming the calibration can be made, set the Time Base Duration switch to 20 μs, but keep the Final Delay set to 90%. Then adjust the value of capacitor C215 (nominally 91 pF), either by replacing it or shunting it, until the required accuracy is attained. If desired, one could go on to check all of the time base durations in an analogous manner. The tolerance in each case is ±5% of full scale and no adjustments are provided.

(6) Turn off the power, separate the Time Base Board from the extender board, and return the Time Base Board to its socket. Turn the power back on.

5.9 SCAN/PULSE (partial)

(1) Set the Initial and Final Delay dials to 0% and 100% respectively. Then set the Delay Mode switch to HOLD.

(2) Connect the DVM to the Scan Delay Output jack (rear panel). Press and hold down the Scan Reset pushbutton. While holding down the button, adjust R317 (SCAN ZERO) for a meter indication of 0 V ±10 mV. Release the pushbutton and verify that the voltage remains at zero.

(3) Set the Scan Rate switch to one minute. Then set the Delay Mode switch to SCAN. The monitored voltage will begin rising. When the indicated voltage is in the range of +1 V to +2 V, set the Delay Mode switch to HOLD. The meter indication should change no more than ±1 mV in the next 60 seconds.

(4) Reduce the setting of the Final Delay dial to 10%. Then set the Repeat/Single switch to SINGLE and the Delay Mode switch to SCAN.

Hold down the Reset pushbutton. The meter should indicate zero. Then release the pushbutton. The indicated voltage should increase linearly to +1 V in six seconds. It should hold at the level and the Tilt light should turn on.

Set the Repeat/Single switch to REPEAT. The indicated voltage should immediately reset to 0 V ±100 mV and begin ramping up to +1 V again. When it reaches +1 V, it will reset again. This reset/ramping sequence will repeat indefinitely.

(5) Set the Final Delay dial to 25%. The ramp amplitude should increase to +2.5 V and the time required to reach this voltage should be 15 seconds. Adjust R1171 if required (R1171 is located on the Preamplifier Board) such that the required time is 15 seconds ±1 second. Then set the Final Delay dial to 100% and readjust R1171 for a +10 V ramp in exactly 60 seconds.

5.10 SIGNAL CONTROL BOARD

(1) Set the Sensitivity switch to 1 V and the Coupling switch to DC. Then connect the power supply, initially set for 0 V output, to the 100 kΩ input of the Model 160.

(2) Begin increasing the power supply voltage. The Model 160 Overload light should come on somewhere in the range of nine to eleven volts. Reset the power supply voltage to zero.

(3) Reverse the polarity of the power supply output. Again increase the voltage until the Overload light turns on, which it should do in the

range of nine to eleven volts. Reset the power supply voltage to 0 V and remove the supply.

(4) Set the front-panel controls as follows.

Coupling switch	GRD.
Aperture Time	100 ns
Offset Polarity	+
Offset Scale	X10
Offset dial	32%

(5) Adjust R538 (HR OVLD ADJ), if required, so that the Overload light is on but right on the threshold of going off.

(6) Set the Offset Polarity switch to OFF.

(7) Set the Trigger Mode switch to CONT. GATE and monitor the Inverted Output jack (rear panel) with the digital voltmeter. Then adjust the front-panel Zero control for a DVM indication of zero volts. If the adjustment resolution is such as to make it impossible to get closer than within a few millivolts of zero, note and record the final voltage.

(8) Transfer the DVM to the Normal Output jack. Then adjust R549 to the same voltage (±5 mV) as was recorded at the end of step 7.

(9) Set the Sensitivity switch to CAL. and adjust R502 (LOOP GAIN ADJ) for a DVM indication of 10.0 ±10 mV. Then set the Sensitivity switch to "10 V" and adjust the front-panel Zero control for zero meter indication. Alternate between the two adjustments (alternating between the CAL. and "10 V" positions of the Sensitivity switch as required) until the 0 V and 10 V readings are as accurate as the control resolution allows. Leave the Sensitivity switch set to CAL.

(10) Note the panel meter indication. If it is not exactly full scale, adjust R568 for full scale meter deflection. NOTE: Early units do not have this adjustment.

(11) Set the front-panel controls as follows.

Trigger Mode	RECURRENT
Time Base Duration	50 µSEC.
Aperture Time	1 µSEC. (high resolution mode)
Blue Time Constant	300 µSEC.
Red Time Constant	.01 mSEC.
Stretch Time	100 µSEC.
Retention	OFF

(12) Alternate between adjusting the front-panel Zero control and R507 (HR GAIN) for 0 V and 10.0 V respectively on the DVM. As in step 9, alternate between the 10 V and CAL. positions of the Sensitivity switch and adjust to within the resolution limits of the contols. Remove the power supply and set the Coupling switch to GRD.

5.11 CHOPPER STABILIZED INTEGRATOR - Do not perform this alignment unless the holding time characteristics of the instrument are suspect.

(1) Turn off the power. Then remove the Integrator Board and mount it in the extender. Mount the combination in the Integrator Board socket. Turn the power back on.

(2) Set the Trigger Mode switch to CONT. GATE. Then jumper the junction of resistors R728 and R757 to ground.

(3) Monitor pin 18 of the Integrator Board with the center-zero dc voltmeter. A convenient sensitivity would be ±20 V full scale.

Adjust R715 for zero meter indication. This is an open-loop adjustment and will probably exhibit considerable instability. If the adjustment is so sensitive that a very minute rotation of R715 causes the meter indication to "smap" from -14 V to +14 V (or vice versa), set R715 at the snap threshold.

(4) Remove the jumper. Then separate the Integrator Board from the extender and return the Integrator Board to its socket.

5.12 SAMPLER AND SCAN/PULSE BOARDS - The following procedure is required only if either the Sampler or the Scan/Pulse Boards have been replaced or extensively repaired. If the sampling circuitry is functioning normally, these adjustments are neither necessary nor desirable.

(1) Turn off the power.

(2) Set the inner dial of the Aperture control to "30".

(3) Note that there are two potentiometers mounted on the Aperture Time switch. In this step we are concerned with the 10 kΩ potentiometer, which is the one closest to the last deck of the switch. Observing this potentiometer, note that the wiper and one of the other two terminals are jumpered together. Connect the ohmmeter (DO NOT USE THE X1 RANGE) between the wiper and the other terminal.

(4) While observing the ohmmeter, begin rotating the inner dial of the Aperture control clockwise. The indicated resistance should decrease down to some minimum. Stop at that minimum. If the dial is turned too far, a series of two or three "minimums" may be noticed to occur in rapid succession. The correct minimum is the one immediately adjacent to the linear resistance region of the potentiometer.

(5) Taking care not to disturb the dial setting as indicated by the ohmmeter, loosen the set screw which secures the inner dial of the Aperture control. Then adjust the position of the dial (the required adjustment should be small) such that "5" is straight up, that is, the "tic mark" for "5" should be directly in line with that indicating

the position of the outer dial. Finally, retighten the set screw and remove the ohmmeter.

(6) Set the front-panel controls as follows.

Trigger Mode	RECURRENT
Initial Delay	50%
Final Delay	100%
Stretch Time	10 µs
Delay Mode	DELAY
Time Base Mode	INT.
Time Base Duration	5 µSEC.
Aperture Time Range	10 nSEC.
Aperture Time Multiplier	"50"

(7) Remove the Sampler Board, mount it in an extender, and return the combination to the Sampler Board socket. Then turn on the power and wait five minutes.

(8) Using the oscilloscope, compare the signal at the junction of R448 and CR412 with that at the junction of R466 and CR417. Both of these signals should be a pulse with a peak-to-peak amplitude in the range of eight to ten volts. Adjust R382 (SYMMETRY adjustment on Scan/Pulse Board) such that the two pulses, except for polarity, are as near identical as possible, with the constraint that the rise and fall times should be kept as fast as possible.

(9) Note that the positive going pulse is referenced to a negative voltage while the negative going pulse is referenced to a positive voltage. Both pulses cross over zero volts. The width for either pulse is measured midway between zero and the peak amplitude of that pulse. Each pulse should have a duration of 50 ns ±2.5 ns as shown in Figure V-9.

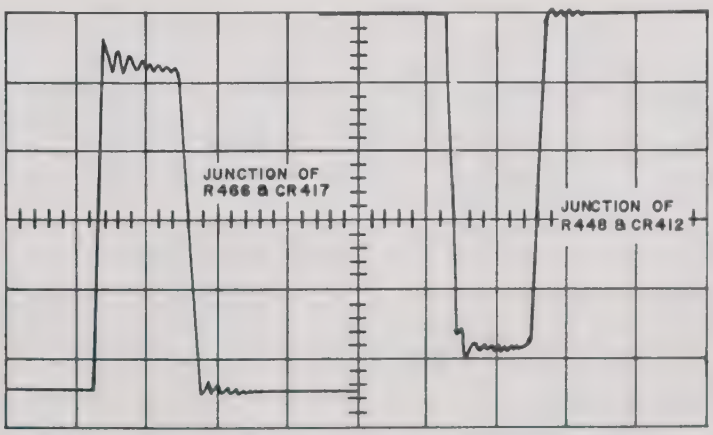


Figure V-9. SAMPLING BRIDGE STROBE PULSES

(10) Set the Aperture Range switch to "1 nSEC." Again note and record the pulse width. It should be 50 ns ±5 ns.

(11) Set the Aperture Range switch to "100 nSEC." Again note and record the pulse width. It should be 5 µs ±250 ns.

(12) A single adjustment, R389 (A. T. CALIBRATE) affects the pulse widths noted in steps 9, 10, and 11. Adjust R389 for the best possible compromise in setting the accuracy of all three pulse durations.

(13) Set R382 (SYMMETRY) to the fully clockwise position. Then connect a jumper from the junction of R462 and R463.

(14) Monitor the voltage at the grey test point with the DVM and adjust R494 (ZERO) for zero indicated voltage. Then disconnect the jumper.

(15) Set the front-panel Retention control to OFF and adjust R382 fully counterclockwise. Note the miniature rotary Test Mode switch mounted on the Sampler Board. It should be in the "straight-up" or 12 o'clock position. Rotate this switch one step counterclockwise, that is, to the 11 o'clock position.

(16) Transfer the DVM to the green test point and set R466 (SAMPLER OFFSET) to the center of its range. Then adjust R458 for as near exactly 0 V at the green test point as is possible to obtain.

(17) Set the Aperture Time switch to "1 µSEC." and connect a jumper between pins 22 and 23 of the Sampler Board. Reset the Test Mode switch to its original position (12 o'clock) and transfer the DVM back to the grey test point. Adjust R403 for a 0 V indication. Then disconnect the jumper.

(18) Turn R382 (SYMMETRY) to the center of its range. Then set the Test Mode switch to 1 o'clock. Reset the Aperture Time Range switch to "10 nSEC."

(19) Compare the signal at the junction of R448 and CR412 with that at the junction of R466 and CR417. Both of these should be a pulse with a peak-to-peak amplitude of approximately 10 V. Adjust R382 (SYMMETRY adjustment on Scan/Pulse Board) such that the two pulses, except for polarity, are as near identical as possible, with the constraint that the rise and fall times should be kept as fast as possible. The pulses should be as shown in Figure V-9.

(20) Reset the Test Mode switch to the normal (12 o'clock) position.

(21) Remove the extender board, separate the Sampler Board from the extender, and return the Sampler Board to its socket.

5.13 INTEGRATOR/GATE BOARD

(1) Set the controls as follows.

Time Base Duration ---------- 10 mSEC.
Aperture Time Range ---------- 10 µSEC.
Aperture Time Multiplier ---------- 10
Initial Delay ---------- 10%

(2) Turn off the power. Then remove the Integrator Gate Board, mount it in the extender, and return the combination to the Integrator Gate Board socket. Turn the power back on.

(3) Monitor pin 12 with the oscilloscope. The observed signal should be +5 V pulse with a duration of 100 µs. Adjust R653 (MIN. GATE ADJ.) for a pulse width of exactly 100 µs.

(4) Set the Aperture Time Multiplier to "50". The duration of the observed pulse should increase to 500 µs. Adjust R650 (MAX. GATE ADJ.) for a pulse duration of exactly 500 µs.

(5) Alternate between adjusting R653 with the Aperture Time Multiplier set to "10" and adjusting R650 with the Multiplier set to "50" until the pulse width is exactly right at these two endpoints.

(6) Set the controls as follows.

Time Base Duration ---------- 2 µSEC.
Aperture Time Multiplier ---------- 10
Aperture Time Range ---------- .1 µSEC. (red)
Initial Delay ---------- 20%
Time Constant (red) ---------- 0.3 mSEC.

(7) Turn off the power. Then remove the Signal Control Board and the Chopper Stabilized Integrator Board.

(8) Connect a 10 kΩ resistor between pin 7 of the Integrator/Gate Board and ground. Then connect a jumper between pin 1 and ground.

(9) Turn on the power and connect the DVM across the 10 kΩ resistor.

(10) Adjust trim-capacitor C600 for 0 V meter indication. Make the adjustment carefully. The final indicated voltage should be less than 100 µV (either polarity).

(11) Turn off the power. Then remove the jumper and the 10 kΩ resistor. Separate the Integrator Gate Board from the extender, remove the extender, and return the Integrator Gate Board to its socket.

(12) Return the Signal Control and Chopper Stabilized Integrator Boards to their sockets.

The alignment is completed. "Button up" the instrument, taking extreme care not to damage the wiring harness when sliding in the bottom cover. Make sure that the slots in the locking bar are properly aligned with the circuit boards before tightening the hold-down screws.

SECTION VI
TROUBLESHOOTING

6.1 INTRODUCTION

Although the Model 160 Boxcar Integrator is a highly reliable instrument, component deterioration or failure could cause the instrument to no longer meet specifications or even to become inoperative. By using the following procedure, a person reasonably familiar with the operation of the Model 160 should be able to isolate the problem to a specific circuit board, or, in many instances, even to a specific circuit. A basic assumption underlying these procedures is that the controls and wiring are not defective. Hence, it could happen that a board indicated as being "defective" is not. and that the problem lies with the wiring or with an associated control. Once the problem is isolated to a specific board, further checks should be conducted to ascertain whether there is a control or wiring problem.

Two characteristics of this troubleshooting procedure are that it is very simple and that no sophisticated test equipment is required. A general purpose multimeter, such as the Simpson 260, is the only required instrument. Most of the checks are of a go/no-go nature. In those cases where the function checked has many ranges, such as the time base duration, the basic check is made at one range only. Usually, this will suffice to check the circuit itself. If the problem is confined to a single range or group of ranges of a multi-range function, chances are that either the switch which selects the ranges or one of its associated components is faulty.

Once the malfunctioning board is located, the user should contact Princeton Applied Research Corporation for advice on the relative merits of repairing the board himself or returning it to the factory for repair or replacement.

Note that the information provided is not oriented toward making a field repair, but only toward identifying a malfunctioning circuit board. However, information provided elsewhere in the manual should prove useful for further troubleshooting. Section IV contains a detailed description of each circuit. Voltage and waveform information is furnished on the schematics at critical points. Other useful drawings include the circuit board location diagram on page V-4, along with the schematics and parts location diagrams in Section VIII. At the end of this section there is a table which defines the voltages and signals at all pins of all the plug-in boards. The appropriate control settings are specified. Attention is called to subsection 6.2, which deals with soldering on printed circuit boards. A few minutes study of this material could prove of value to those who, although experienced in conventional soldering techniques, have not worked with printed circuit boards.

6.2 PRINTED CIRCUIT SOLDERING

If any components are removed from the printed circuit boards for inspection or replacement, be especially careful not to damage the print. To remove components cleanly requires considerable care. Either one of two methods can be used to remove the solder from the pad. The first entails use of a vacuum-

bulb type solder remover and the second use of a "wick". Both methods give good results. A brief description of each follows.

METHOD ONE

Removing solder by means of a solder remover is a straightforward, relatively simple process. The required equipment includes a vacuum-bulb type solder remover (UNGAR SOLDER-OFF #7805 recommended) and a good soldering iron of moderate power (WALL type 14HDG40120 with a type W14KS tip). To remove a component, proceed as follows.

Heat the pad on the side opposite the component. As soon as the solder flows, use the solder remover to remove the solder from the pad and hole. Take care not to prolong the heating any longer than necessary. After the solder has been removed, straighten the lead. If enough solder has been removed to "free" the lead, pull the lead through the hole from the component side of the board, using suitable long-nose pliers. If the lead is not free, continue to apply heat while pulling the lead until the lead comes free. In the case of components whose leads cannot be removed one at a time, such as trim-potentiometers, use the solder remover to free all of the leads before attempting to pull the component from the board. If it is not possible to completely free all of the leads, the component can be removed by first applying heat to one lead, followed by rocking the component to pull that lead through as far as possible, and then gsuccessively repeating the process for each of the other leads. By repeating the "heating-and-rocking" process, the component will eventually come free. After the component has been removed, use the solder remover to completely clear the solder from the holes.

METHOD TWO

Wicking entails using a length of stranded wire or shielding braid as a wick to draw up the molten solder from the pad. With this method, exceptionally clean work is easily achieved. Equipment required includes a good soldering iron (that recommended in method one is excellent), a supply of stranded wire or shielding braid, and some rosin base soldering flux (ALPHA 346-35, or equivalent).

Dip a few inches of stranded wire (shielding braid is ideal) into the rosin-base soldering flux. Then place the wire or braid on top of the joint to be unsoldered, allowing some of the flux to flow over the joint. NOTE: Under no circumstances use an acid base flux.

As shown in Figure VI-1, place a hot soldering iron on top of the stranded wire directly above the joint to be unsoldered. Within a few seconds, most of the solder in the joint will flow quickly up the wick, leaving the joint area free of solder.

Lift the soldering iron and remove the wick before it freezes to the joint. Cut off the "filled" end of the wick (generally about ½ inch should be removed).

Inspect the joint. If any solder remains, repeat the procedure as required. Then straighten the lead and, while applying heat to keep the solder in the

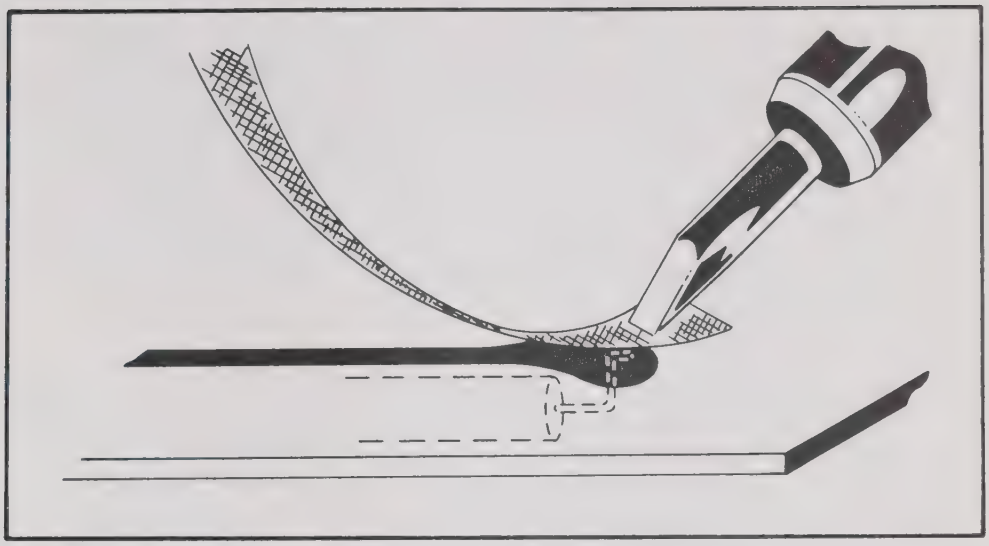


Figure VI-1. SOLDER REMOVAL BY WICKING

hole molten, pull it through the hole. Components with leads which cannot be removed one at a time can be removed by the "heat-and rock" technique described earlier. After the component has been removed, use wicking to completely clear all solder from the holes.

INSTALLING COMPONENTS

Before returning a component or its replacement to the board, make sure the leads are bent on the proper centers and that they don't angle in or out. If they do not pass freely through the centers of the holes, they may catch the edge of the print and lift it. Bend and cut the leads after inserting the component. Solder the leads with a hot iron (no larger than 40 watts) and a good grade of rosin core 60/40 solder. Be sure to apply heat no longer than necessary to achieve a good joint (usually a few seconds with a clean properly tinned iron). After soldering, clean the board with flux remover (ALPHA 653 or equivalent). NOTE: No harm will result from leaving the flux on the board other than to degrade its appearance. Using these techniques, no damage to the board or print will take place and, after completion of the job, the board will be indistinguishable from one which is "fresh from the factory".

6.3 PRELIMINARY STEPS

(1) Remove the top and bottom covers.

(2) It may be advantageous to operate the instrument on its side, particularly if one intends to check the signals and voltage levels at the pins of the plug-in boards. Alternatively, one would have to use Extender Boards.

(3) The gating device in the normal resolution mode is an insulated gate

type field-effect transistor, Q600, located on the Integrator Gate Board. This transistor has been carefully selected to a stringent leakage specification. Although this transistor is mounted in a socket, the user is cautioned against removing this transistor for any reason because of its susceptibility to being damaged by static electricity. If the transistor is removed, use considerable caution, particularly with regard to touching the gate lead. By holding the case firmly, no significant potential can exist between the gate and other leads if the gate lead is touched accidentically. If the transistor should ever fail, it will be necessary to order the replacement transistor from the factory. Equal care must be exercised in handling the replacement.

(4) Special attention is called to the reed relays, of which there are 22 in the Model 160. Although rugged enough to last indefinitely in normal service, these components are susceptible to damage when the boards are removed. One must be particularly careful not to flex a circuit board as this could easily crack a relay. Such damage is not always easily detected because the relays are almost entirely hidden inside their energizing coil; intermittent troubles or erratic instrument performance are frequently the result of cracked relays. Table VI-1 lists all of the reed relays and shows the required conditions for energizing in each case.

6.4 POWER SUPPLY CHECKS

(1) Turn the power on. Then check the voltage at the following Power Supply Board test points.

Red Test Point	+24 V
Blue Test Point	+12 V
White Test Point	-12 V
Yellow Test Point	-24 V

(2) Measure the voltage at pin 3 of the Power Supply Board. The indicated voltage should be +4.5 V.

(3) Measure the voltage at pin 22 of the Chopper Stabilized Integrator Board. The indicated voltage should be approximately -200 V.

If the voltages measured in steps one through three were as indicated, go on to subsection 6.5. If abnormal indications were noted, the problem could lie with one of the regulators or even with the unregulated supply circuitry. Do not overlook the possibility of a short circuit somewhere else in the instrument.

In checking the unregulated supply circuitry one could check the ripple on the various filter capacitors. Any general purpose oscilloscope could be used. The appropriate pins of the Power Supply Board can be used as monitor points. Typical pk-pk ripple levels are indicated at the top of page VI-6. These levels, and the dc levels, are approximate.

Relay	Where Located	Energize Condition
S1100*	Preamplifier Board	Application of bar magnet (for alignment only).
S1101*	Preamplifier Board	Application of bar magnet (for alignment only).
K100	Trigger Board	Time Base Mode switch to EXT.
K200	Time Base Board	Time Base duration of .1 mSEC or longer.
K201	Time Base Board	Time Base Mode switch to INT.
K300	Scan/Pulse Board	Scan Ramp in progress or HOLD.
K301	Scan/Pulse Board	Scan Ramp not in progress (in act of resetting or disabled at end of scan in single scan operation).
K302	Scan/Pulse Board	Aperture Time Range switch set to 10 nSEC.
K303	Scan/Pulse Board	Aperture Time Range switch set to 100 nSEC.
K401	Sampler Board	Fast (blue) Time Constant switch set to 3 nSEC, 10 nSEC, 100 nSEC, 1 µSEC, 3 µSEC, 30 µSEC, or 300 µSEC.
K402	Sampler Board	Fast (blue) Time Constant switch set to 3 nSEC, or 1 µSEC.
K403	Sampler Board	Fast (blue) Time Constant switch set to any position in range of 100 nSEC through 1000 µSEC.
K404	Sampler Board	Fast (blue) Time Constant switch set to any position in range of 30 µSEC through 1000 µSEC.
K405	Sampler Board	Fast (blue) Time Constant switch set to 1 µSEC, 3 µSEC, 10 µSEC, 300 µSEC, or 1000 µSEC.
K501	Signal Control Board	High Resolution Mode operation.
K502	Signal Control Board	Normal Resolution Mode operation
K600	Integrator Gate Board	Time Constant (red) switch set to .01 mSEC.
K601	Integrator Gate Board	Time Constant (red) switch set to any position in range of .1 mSEC through 3 SEC.
K602	Integrator Gate Board	Time Constant (red) switch set to 10 SEC.
K603	Integrator Gate Board	Time Constant (red) switch set to 30 SEC.
K604	Integrator Gate Board	Time Constant (red) switch set to 100 SEC.
K701	Chopper Stabilized Integrator Board	Reset Pushbutton depressed.

*These are reed switches without energizing coils.

Table VI-1 MODEL 160 REED RELAYS, THEIR LOCATION AND ENERGIZING CONDITION FOR EACH

Capacitor Checked	Pin	DC Level	Pk-Pk Ripple
C22	1	+9 V	0.5 V
C19	7	-32 V	0.7 V
C18	13	+32 V	0.8 V
C20	16	+19 V	0.4 V
C21	22	-19 V	0.4 V

The unregulated high voltage is checked at the negative end of capacitor C10, which is located on the Rectifier Board. The voltage across this capacitor is typically -310 V and the ripple is typically 10 V pk-pk.

6.5 LOGIC AND TIMING CIRCUITS

TIME BASE GENERATOR (Time Base Board)

(1) Set the front-panel controls as follows.

Time Base Duration	20 SEC.
Time Base Mode	INT.
Trigger Mode	RECURRENT
Initial Delay	5%
Final Delay	100%
Scan Mode	DELAY
Aperture Time Range	100 µSEC.
Aperture Multiplier	10

(2) Monitor the Time Base Output jack (rear panel) with the voltmeter. One should observe successive positive ramps (0-to-10 V) with a repetition period of 20 s. If the indicated behavior is noted, the Time Base Generator circuit (Q214 through Q219 on the Time Base Board) is functioning normally. If the behavior is abnormal, the problem could lie with the Time Base Generator or with one of the circuits which generates the logic inputs to the Time Base Generator. These are checked in step 3.

(3) Monitor the dc voltage at pin 23 of the Time Base Board. It should be approximately +3 V. If this voltage is abnormal, a Trigger Board circuit is probably malfunctioning.

Monitor the dc voltage at pin 22. The measured voltage should be within a half volt of ground. If it is not, a circuit on the Integrator Gate board is causing the problem.

Measure the dc voltage at pin 21. In instruments not having analog storage, this voltage will be +4.5 V. In the case of instruments equipped with the analog storage option, the voltage should be at least 2.5 V. If it is not, the Analog Storage Board circuit is malfunctioning.

If all three of these logic voltages checked normal, and if the indicated ramps are not present at the Time Base Output jack, the Time Base Generator circuit is the most likely source of trouble.

DELAY SCAN BUFFER (Scan/Pulse Board)

(1) Set the Scan Mode switch to DELAY.

(2) Monitor the Scan/Delay Output jack (rear panel) with the dc voltmeter. Then vary the Initial Delay dial over its entire range. The voltage at the Scan/Delay Output jack should vary linearly with the dial setting and reach a maximum of +10 V when the dial is fully clockwise. When the dial is fully counterclockwise, the voltage should be zero. Leave the Initial Delay dial set to 5%.

If the indicated behavior was noted, the Scan Delay Buffer circuit (A301 and associated components on the Scan/Pulse Board) is functioning normally. If abnormal indications are observed, this circuit is faulty.

DELAY SCAN GENERATOR (Scan/Pulse Board)

(1) Set the Scan Rate switch to "1 MIN.", the Repeat/Single switch to REPEAT, and the Scan Mode switch to SCAN.

(2) Monitor the Scan/Delay Output jack (rear panel) with the dc voltmeter. One should observe successive positive ramps (0-to-10 V) with a repetition period of one minute. If the indicated behavior is noted, the Scan Generator circuit (Q300 through Q306 on the Scan/Pulse Board) is functioning normally. If the indicated behavior is not observed, this circuit is faulty.

$E_f > E_i$ DETECTOR
AND TILT LAMP DRIVE (Scan/Pulse Board)

(1) Set the Initial Delay dial to 90%, the Final Delay dial to 80%, and the Scan Mode switch to DELAY. The Tilt Lamp should turn on. If it does, the Scan Finish Detector circuit (Q309 through Q315 on the Scan/Pulse Board) and the Tilt Lamp Drive circuit (Q611-Q612 on the Integrator Gate Board) are functioning normally. If it does not, one of these circuits is probably malfunctioning. Do not overlook the possibility of a burned out indicator lamp.

(2) Reset the Final Delay dial to 100% (the Tilt light should go out) and the Initial Delay dial to 10%.

NORMAL RESOLUTION
MODE MONOSTABLE

(1) Set the Time Base Duration at 0.1 ms.

(2) Set the Aperture Time Range selector to "1 mSEC." and the Aperture Time Multiplier to 45.

(3) Monitor the Gate Out jack (front panel) with the dc voltmeter. The voltmeter reading should be between 0 V and +2 V. If the Aperture Time Multiplier is turned clockwise, the voltage will decrease. If it is

turned counterclockwise, the voltage will increase. In this measurement, the meter simply indicates the average dc at the Gate Out jack. This average in turn is a function of the gate pulse amplitude, duration, and repetition rate. For more precise confirmation of proper monostable operation, one could monitor the output with an oscilloscope.

(4) Set the Trigger Mode switch to EXT. The dc voltage should decrease to approximately -0.6 V, indicating that the monostable is not "firing".

(5) Set the Trigger Mode switch to CONTINUOUS. The indicated voltage should be approximately +2.5 V.

(6) If the indicated results were obtained in the preceding steps, one can be reasonably sure that the NR Monostable and the circuits between the output of that monostable and the Gate Out jack are all functioning normally. If abnormal indications are obtained, one of these circuits is malfunctioning. These circuits are located on the Integrator Gate Board.

HIGH RESOLUTION MODE
MONOSTABLE, GATE STROBE
AMPLIFIER, AND TILT LAMP DRIVER

(1) Set the Aperture Time Range switch to "100 nSEC." (blue) and the Aperture Multiplier to 12. Set the Stretch Time at 10 μs. Select a time base duration of 2 μs.

(2) Continue to monitor the dc voltage at the Gate Output jack. As before, the voltage in the continuous mode should be approximately +2.5 V. In the recurrent mode it should be in the range of 0 V to +2 V, and in the external mode it should be approximately -0.6 V.

(3) These checks are exactly anologous to the immediately preceding NR Monostable checks. If the voltages are as indicated, one can be reasonably sure that the HR Monostable (Scan/Pulse Board) is functioning normally, as is the first stage of the Gate Strobe Amplifier (Sampler Board) and the HR Tilt Driver (Sampler Board). Those Integrator Gate Board circuits which are between the "Strobe Pulse Input" to that board and the "Gate Output" must also be working properly. If improper voltages are noted, one of these circuits is malfunctioning. Signal tracing with an oscilloscope will be required to identify which of the circuits is causing the problem.

TILT LAMP FLASHER

(1) Set the Trigger Mode switch to RECURRENT and the Aperture Time Range switch to "10 mSEC." The Tilt light should commence flashing at an approximate rate of two times per second, indicating that the Tilt Lamp Flasher circuit (Q609 and Q610 on the Integrator Gate Board) is functioning normally. If the light does not flash as indicated, this circuit is malfunctioning.

(2) Set the Trigger Mode switch to EXT. The Tilt light should go out.

EXTERNAL TRIGGER

(1) Set the Slope switch to "-" and turn the Threshold control fully counterclockwise.

(2) Slowly turn the Threshold control clockwise. The Tilt light should flash once as the Threshold control passes through the center of its range. Leave the Threshold control fully clockwise.

(3) Set the Slope switch to "+". The Tilt light may or may not flash when the setting of the Slope switch is changed.

(4) Begin turning the Threshold control counterclockwise. The Tilt light should flash once as the Threshold control passes through the center of its range.

(5) If the indicated behavior was noted, one can be reasonably sure that the External Trigger circuitry is functioning normally. This circuitry, which includes the Trigger Input circuit, the Trigger Shaper circuit, and the Slope and Trigger Mode Detect circuit, is located on the Trigger Board. If abnormal behavior is noted, one of these circuits is probably malfunctioning.

DELAYED TRIGGER

(1) Set the Time Base Duration to "20 SEC." and the Output Trigger Delay dial to 50% (Delayed Trigger Mode switch* to DIAL).

(2) Load the Delayed Trigger Out jack with 50Ω. Then monitor the Delayed Trigger Out jack with the dc voltmeter. The indication should be approximately 0 V.

(3) Set the Trigger Mode switch to RECURRENT while continuing to monitor the Delayed Trigger Out jack. The dc voltage should remain at 0 V for approximately 10 seconds, and then rise to about +1½ V for the next ten seconds. These alternate 10 second periods of 0 V and +1½ V should repeat indefinitely.

(4) Set the Trigger Mode switch to EXT. to stop the process. The pedestal in progress will finish.

(5) If the indicated results were obtained, the Delayed Trigger circuitry (Trigger Board) is functioning normally. Conversely, improper indications show the circuit to be faulty.

*This switch not provided in early units.

6.6 SIGNAL FLOW

PREAMPLIFIER ZERO

(1) Set the Input Sensitivity to "100 mV" and the Offset Polarity switch to OFF.

(2) Monitor the Preamplifier Output jack (rear panel) with the voltmeter. The meter should indicate 0 V ±50 mV. If it does, the Preamplifier zero is within tolerance. If it does not, the zero is out of tolerance, indicating a possible Preamplifier malfunction or need for realignment.

PREAMPLIFIER GAIN

(1) While continuing to monitor the voltage at the Preamplifier Output jack, set the Sensitivity switch to CAL.

(2) The indicated voltage should be -0.5 V ±50 mV* (assuming the meter has a sensitivity of 20,000 ohms per volt or better).

(3) If the voltage measured was in tolerance, the Preamplifier is probably functioning normally. If not, a possible malfunction or need for realignment is indicated.

INPUT OFFSET (X1)

(1) Set the Input Offset Scale switch to X1. Then set the Input Offset dial fully clockwise.

(2) Set the Input Offset Polarity switch to "-". The Voltmeter (still monitoring the Preamplifier Output jack) should indicate 0 V ±50 mV, indicating that the network which determines the offset voltage in the "-" position is within tolerance.

INPUT OFFSET (X10)

(1) Set the Sensitivity switch to "10 V" and the Offset Scale switch to "X10".

(2) The voltmeter should indicate +5 V ±0.5 V.

(3) Set the Offset Polarity switch to "+". The voltmeter should indicate -5 V ±0.5 V.

(4) These steps checked the X10 Offset network and also provided additional Preamplifier checks.

OVERLOAD INDICATOR

(1) Set the Aperture Range switch to "100 nSEC." (blue) and the Trigger

* -1.0 V ±100 mV on early units.

Mode switch to EXT. The Overload light should be on.

(2) Begin slowly rotating the Input Offset dial counterclockwise. The Overload light should go out with an Offset dial setting somewhere between 25% and 40%. Leave the dial fully counterclockwise.

(3) Set the Offset Polarity switch to "-". Then begin rotating the Offset dial clockwise. The Overload light should turn on with a dial setting in the range of 25% to 40%. Leave the dial set to approximately 70%.

(4) Set the Aperture Time Range switch to "1 mSEC." The Overload light should go out.

(5) Set the Sensitivity switch to 0.5 V and the Delay Mode switch to SCAN.

(6) Then connect the Scan/Delay Output signal (rear panel) to the 100 kΩ Signal Input jack (front panel).

(7) Set the Input Offset Polarity switch to OFF.

(8) Hold down the Scan Reset pushbutton.

(9) At some convenient time, release the pushbutton. Approximately thirty seconds later the Overload light should turn on. Disconnect the cable.

(10) The preceding series of steps check the Overload circuit (Signal Control Board) for both high resolution and normal resolution operation. If proper indications were noted, the circuit is functioning normally. If the behavior was other than as indicated, the circuit is faulty.

INTEGRATOR AND INTEGRATOR GATE

(1) Set the controls as follows.

Trigger Mode	EXT.
Time Base Duration	2 µSEC.
Initial Delay	10%
Final Delay	90%
Delay Mode	DELAY
Aperture Time Range	1 µSEC.
Aperture Time Multiplier	10
Time Constant (red)	.01 mSEC.
Input Sensitivity	10 V
Memory	OFF

(2) Connect the voltmeter to the Inverted Output jack.

(3) Momentarily depress the Integrator Reset pushbutton (not the Scan Re-

set pushbutton). The meter should indicate 0 V ±100 mV. If it does not, the problem most likely lies with the chopper stabilized integrator or with the field-effect transistor Normal Resolution gate. The latter can be eliminated by removing the Integrator/Gate Control board and repeating the measurement, taking care to depress the Integrator Reset pushbutton again. If the indication is normal, the Integrator and gate are probably good. The following steps provide additional checks of these and other circuits.

PRE-GATE BUFFER (Signal Control Board)

(1) Set the Trigger Mode switch to CONT. GATE and the Input Offset Polarity switch to OFF.

(2) Connect the voltmeter to the Inverted Output jack.

(3) Momentarily depress the Integrator Reset pushbutton (not the Scan Reset pushbutton). The meter should indicate 0 V ±100 mV. If it does not, the problem most likely lies with the chopper stabilized integrator or with the field-effect transistor Normal Resolution gate. The latter can be eliminated by removing the Integrator/Gate Control board and repeating the measurement, taking care to depress the Integrator Reset pushbutton again. If the indication is normal, the Integrator and gate are probably good. The following steps provide additional checks of these and other circuits.

PRE-GATE BUFFER (Signal Control Board)

(1) Set the Trigger Mode switch to CONT. GATE and the Input Offset Polarity switch to OFF.

(2) While continuing to monitor the Inverted Output with the voltmeter, adjust the Zero Control through its entire range. The voltmeter indication should track the Zero Control setting and should range from more than -10 V to more than +10 V. Note the panel meter indication. It should also track the voltmeter indication. The panel meter indication should be the same magnitude as the voltmeter indication, but of opposite polarity. Leave the Zero control set for a voltmeter (and panel meter) indication of zero.

(3) If the indicated behavior was noted, one can be reasonably sure that the Pre-gate Buffer, the Integrator, and the Output Buffer are all functioning normally. The two Buffer amplifiers are located on the Signal Control Board. If the voltmeter indications were normal but not the panel meter indications, the Output Buffer is faulty. A malfunction in the Pre-gate Buffer circuitry would cause both meters to yield "wrong" indications. If the Gate transistor (Q600 on the Integrator/Gate Board) were not conducting (in the Continuous Trigger Mode the Gate should be locked into conduction), the meter indications would not respond to the Zero control.

HOLD TIME CHECK (Integrator and Gate)

(1) Set the Offset Polarity switch to "+" and the Offset Scale switch to "X1".

(2) Turn the Offset dial to the 50% position. The Model 160 panel meter should indicate positive half scale.

(3) Set the Trigger Mode switch to EXT. Then set the Offset Polarity switch to "-" and note the panel meter indication. Over a period of 100 s the meter indication should deviate from full scale by no more than 10% of full scale.

(4) Set the Trigger Mode switch to CONT. GATE. The panel meter indication should be negative half scale.

(5) Set the Trigger Mode switch to EXT. and the Offset Polarity switch to "+". Observe the panel meter over a period of 100 s. Its indication should change no more than 10% of full scale.

(6) Set the Offset Polarity switch to OFF and the Trigger Mode switch to CONT. GATE. The meter indication should return to zero. If the indicated results were obtained in this series of steps, the Gate (Q600) and the chopper stabilized integrator are functioning normally. If abnormal indications were noted, chances are the gate transistor's "off" resistance has become degraded, or that the Integrator has become defective.

FAST SAMPLER CHECK (Sampler Board)

(1) Connect a cable between the Delayed Trigger Output jack and the 50Ω Input jack.

(2) Set the controls as follows.

Trigger Mode	RECURRENT
Output Trigger Delay	20%
Output Trigger Delay Mode*	DIAL
Time Base Range	2 µSEC.
Time Base Mode	INT.
Initial Delay	5%
Final Delay	40%
Scan Rate	5 MIN.
Delay Mode	SCAN
Aperture Time Range	1 nSEC.
Aperture Time Multiplier	10
Repeat/Single	SINGLE
Time Constant (blue)	30 nSEC.
Time Constant (red)	.01 mSEC.
Retention	mid-range

*Not present in early units.

Stretch Time ---------- 30 µSEC.
Prefilter ---------- OFF
Input Coupling ---------- GRD.
Input Sensitivity ---------- 10 V
Input Selector ---------- 100 kΩ
Offset Polarity ---------- OFF

(3) Adjust the Zero control for an indication of exactly "0" on the panel meter.

(4) Set the Input Sensitivity switch to CAL. and adjust the Retention control for exactly full scale meter indication. Repeat steps (3) and (4), as required.

(5) Set the Sensitivity switch to 2 V, the Coupling switch to DC, and the Input Selector to 50Ω.

(6) Momentarily depress the Scan Reset pushbutton and observe the panel meter. The reading should hold at near zero for approximately one minute, then increase suddenly to approximately +1.2 V. The reading should hold constant at that reading. After approximately two minutes from the time the pushbutton was depressed and released, the Tilt light should turn on.

(6) This series of steps checks almost all of the instrument's circuits. However, most of these have already been checked. Those circuits used for the first time in this series of checks include the Sampler Input Buffer, the Fast Sampler, the second stage of the Gate Strobe Amplifier, and the Sampler Output Buffer. All of these circuits are located on the Sampler Board.

This completes the troubleshooting procedure. Assuming all the boards checked good, one can draw either of two conclusions. First, it is possible that the malfunction is beyond the scope of this troubleshooting procedure. Second, the instrument may be functioning normally, but the operator misunderstands its use or expected behavior in the particular situation of interest. In any case, contact the factory or a factory authorized representative for further advise.

Control Settings		Symbols
Trigger Mode	RECURRENT	↑ = switching "+" to
Output Trigger Delay	50%	↓ = switching "−" to
Slope	+	→ = ramping to
Threshold	center of range	> = greater than
Trigger Input	not connected	* = within one volt of zero
Delayed Trigger Output	not connected	NC = no connection
Delayed Trigger Mode**	DIAL	
Time Base Range	1 SEC.	
Time Base Mode	INT.	
Initial Delay	10%	
Final Delay	90%	
Scan Rate	1 MIN.	
Delay Mode	DELAY	
Repeat/Single	REPEAT	
Aperture Time Range	100 nSEC. (blue)	
Aperture Time Multiplier	50	
Stretch Time	10 μSEC.	
Time Constant (blue)	3 nSEC.	
Retention	OFF	
Time Constant (red)	.01 mSEC.	
Prefilter	OFF	
Input Coupling	AC	
Input Sensitivity	50 mV	
100 kΩ Input	not connected	
Input Selector	100 kΩ	
50 Ω Input	not connected	
Memory	OFF	
Zero	center of range (ten turns)	
Offset Scale switch	X1	
Offset Polarity	OFF	
Offset dial	fully counterclockwise	
Gate Output	not connected	
Power	on (up)	
Output	not connected	

**Not provided in early units.

Board Pin	Trigger Board	Time Base Board	Scan Pulse Board	Sampler Board	Sig. Con. Board	Int. Gt. Board	Int. Amp. Board	Power Board	Preamp. Board
1	0	-24	*↑9	*	0	*	0	9	0
2	*↑2.5	24	1	0	*	24	0	4.5	0
3	0	9	*	*	0	0	*	4.5	0
4	4.5	9	0	0	*	0	0	0	NC
5	-24	-12	0	0	0	0	NC	-32	NC
6	10	0	-1	0	*	0	0	-2.5	NC
7	12	*↑3	*	24	NC	*	NC	-32	0
8	24	0	*→9	24	0	0	NC	0	0
9	*	3↓*	*↑3	0	24	-24	NC	-24	24
10	-12	1	1	0	*	*	0	32	-24
11	0→9	12	9	24	*	*	-24	25	-12
12	0	0	24	-12	*	*	-24	24	12
13	*	0→9	-12	-24	*	*	0	32	0
14	0	*	12	0	24	0	0	0	*
15	4.5	24	-24	0	0	4.5	24	13	0
16	0	-24	2↓*	-3	24	-24	24	19	0
17	3	0→9	0	0	-24	-12	*	12	0
18	0	*	-3	-3	*	24	*	0	0
19	0→9	*	-3	0	0	12	0	0	*
20	0	4.5	0	12	*	12	NC	-19	0
21	*	>2.5	24	*	*	0	NC	-13	NC
22	0	*	24	0	*	24	0	-19	3.4
23	*	3	-17	*	*	2.2↓*	-200	-12	45 mV
24						0			
25						1.4			
26						0			
27						14			
28						0			
29						*			
30						24			
31						0			
32						0			
33						*			
34						0			
35						*			

Table VI-2. TROUBLESHOOTING VOLTAGES AND WAVEFORMS

SECTION VII
WARRANTY

Princeton Applied Research Corporation warrants each instrument of its own manufacture to be free from defects in material and workmanship. Obligations under this Warranty are limited to replacing, repairing or giving credit for the purchase price, at our option, of any instrument returned prepaid to our factory for that purpose within ONE year of delivery to original purchaser. Instruments returned to the factory are accepted only when prior authorization has been given by an authorized representative of Princeton Applied Research Corporation.

This Warranty shall not apply to any instrument, which our inspection shall disclose to our satisfaction, to have become defective or unworkable due to abuse, mishandling, misuse, accident, alteration, negligence, improper installation, or other causes beyond our control.

Princeton Applied Research Corporation reserves the right to make changes in design at any time without incurring any obligation to install same on units previously purchased.

This Warranty is in lieu of, and excludes all other warranties or representations, expressed, implied or statutory, and all other obligations or liabilities of Princeton Applied Research Corporation including special or consequential damages, and no other source is authorized to assume for Princeton Applied Research Corporation any other liability.

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SCHEMATICS

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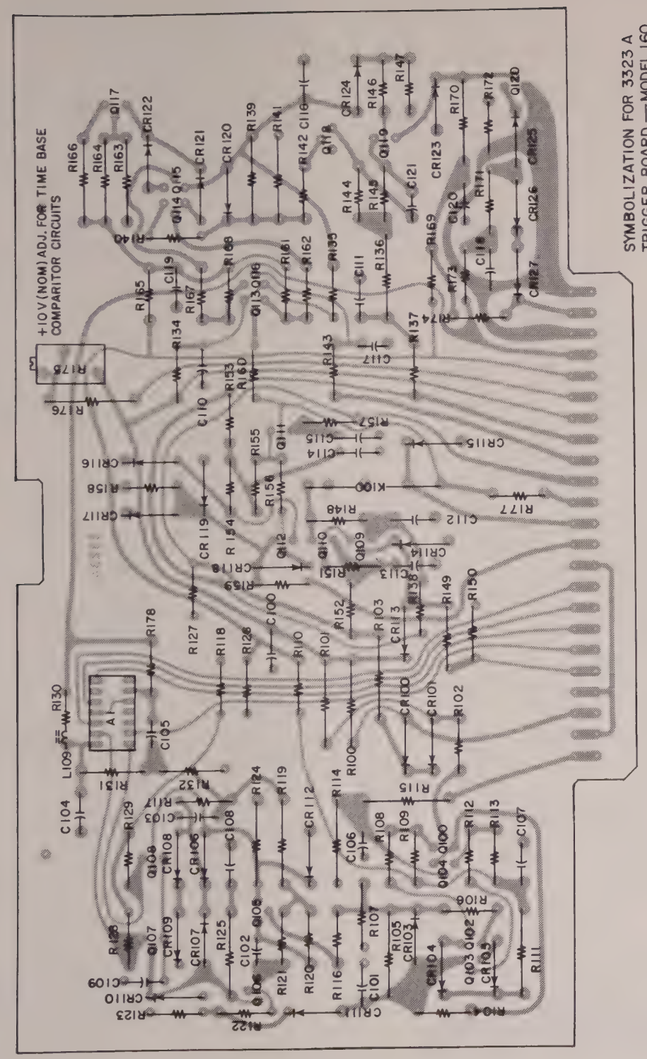

SYMBOLIZATION FOR 3323 A TRIGGER BOARD — MODEL 160

TRIGGER INPUT DETECTOR

SHAPER

TRIGGER SLOPE DETECTOR

A1 IS SN74H00N

VOLTAGES AND WAVEFORMS MEASURED UNDER THE FOLLOWING CONDITIONS

TRIGGER MODE	EXT.
TIME BASE MODE	INT.
TIME BASE RANGE	100 µs
INITIAL DELAY	40%
FINAL DELAY	100%
SCAN MODE	DELAY
DELAY TRIGGER	50%
DELAY TRIGGER SWITCH	DIAL
TRIGGER SLOPE	MINUS
TRIGGER THRESHOLD	"one o'clock"

EXTERNAL TIME BASE BUFFER AMPLIFIER

TIME BASE OUTPUT BUFFER AMPLIFIER

DELAYED TRIGGER CIRCUITRY

NOTES

1. ALL RESISTOR 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. MF INDICATES 1/2W, 0% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. TRANS. Q100-Q104, Q102-Q103, Q113-Q116, Q114-Q115 ARE MATCHED PAIRS PER RAR SPEC. 680415.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
RET.	DELAY TRIG	RET.	+4.5V	-24V	+10V REF	+12V	+24V	DELAY TRIG	-12V	IN/OUT TB	ENABLE TB	TB OUT	STK GND	SLOPE TRIG	MODE TRIG	TB TRIG	SLOPE TRIG	EXT. TB	STK GND	INPUT TRIG	STK GND	BIAS TRIG

PIN CONNECTIONS

TRIGGER BOARD
MODEL 160

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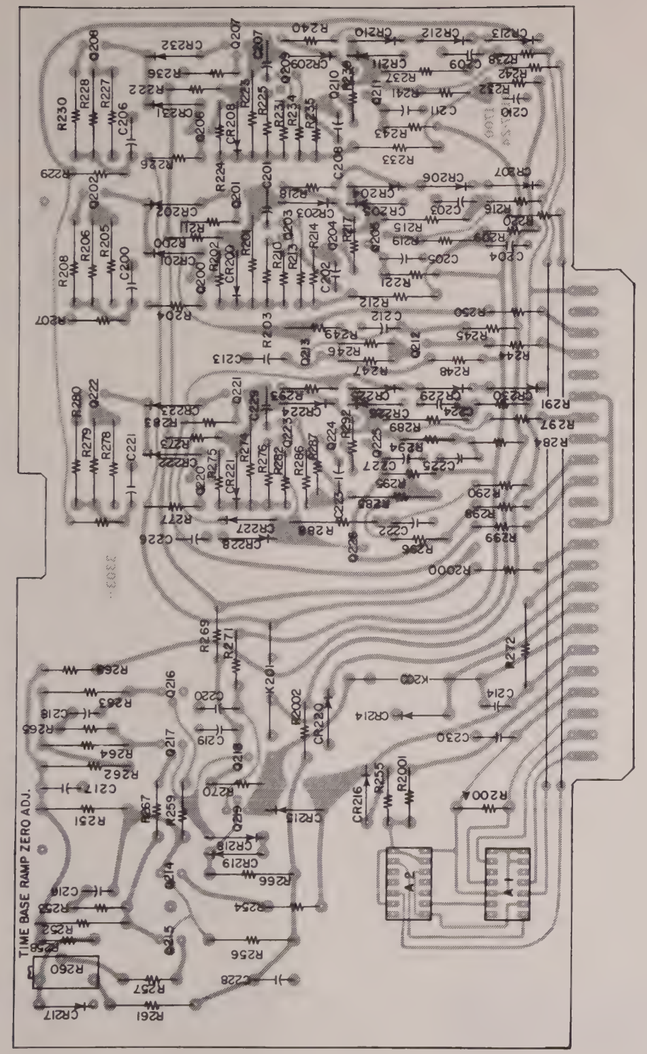

SYMBOLIZATION FOR 3303 B
TIME BASE BOARD — MODEL 160

TIME BASE VERSUS Ef (FINAL DELAY) COMPARITOR

TIME BASE VERSUS ZERO COMPARITOR

Ef (FINAL DELAY) BUFFER AMPLIFIER

≈ +10V at Ef = 100%

TIME BASE VERSUS f(EI) COMPARITOR

TIME BASE GENERATOR

A1 IS SN74H10N
A2 IS SN74H00N

VOLTAGES AND WAVEFORMS MEASURED UNDER CONDITIONS INDICATED ON TRIGGER BOARD SCHEMATIC.

NOTES

1. ALL RESISTORS 1/4W 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. MF INDICATES 1/2W 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. Q214 – Q215 MATCHED PAIR. SPEC. 680425.

TIME BASE BOARD — PIN CONNECTOR — MODEL 160

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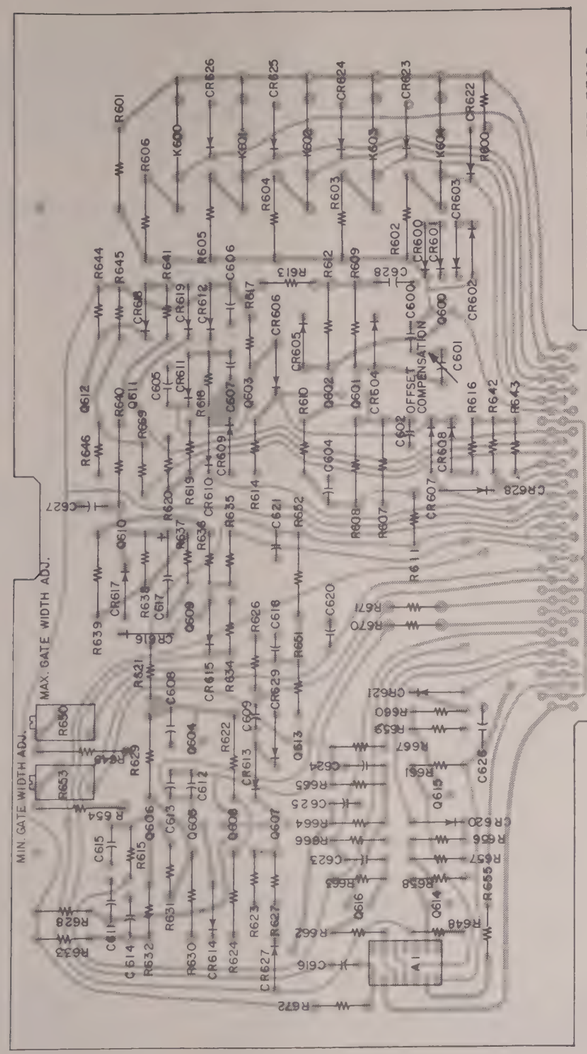
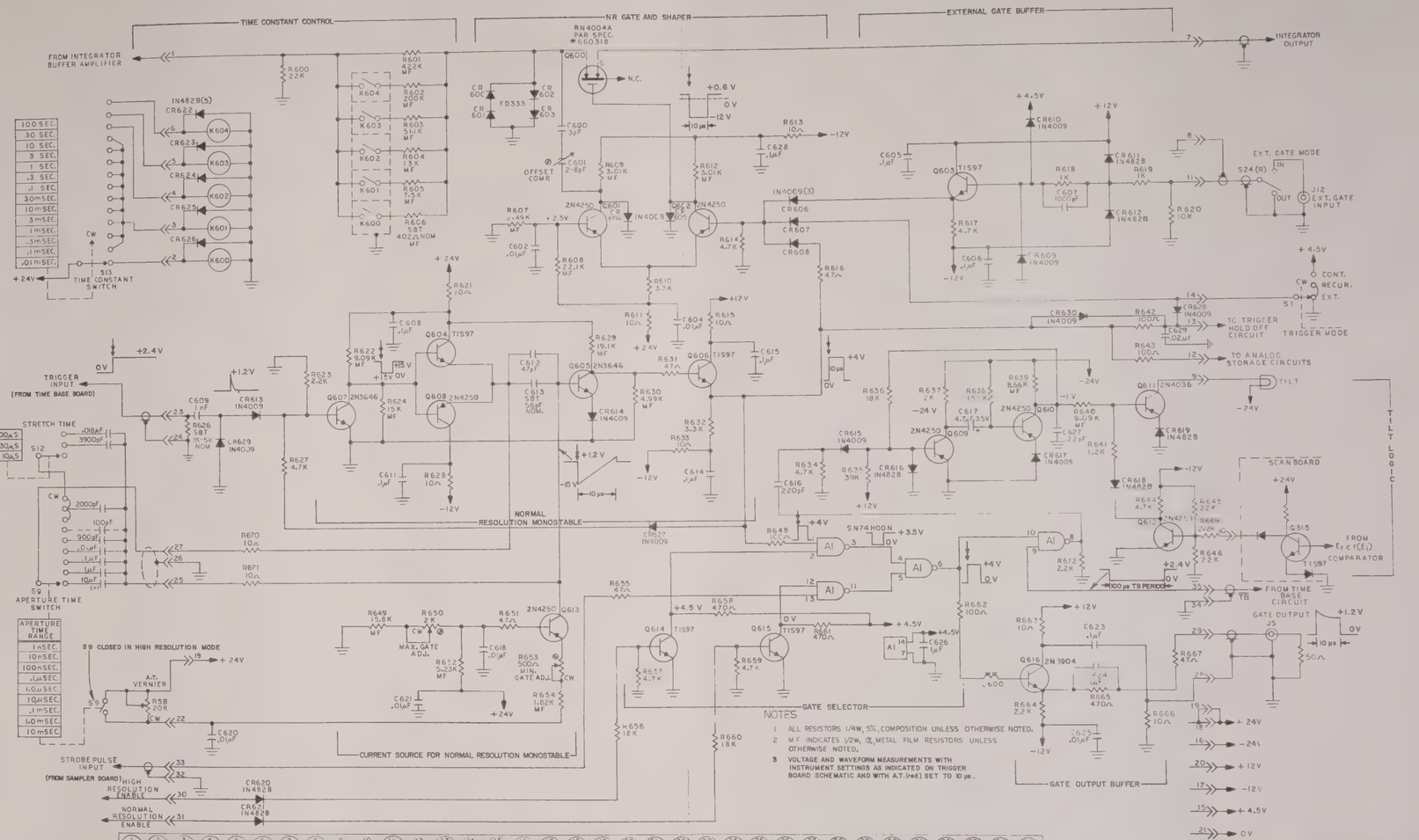
SYMBOLIZATION FOR 3369 D
INTEGRATOR GATE CONTROL BOARD
MODEL 160





INTEGRATOR GATE CONTROL — MODEL 160

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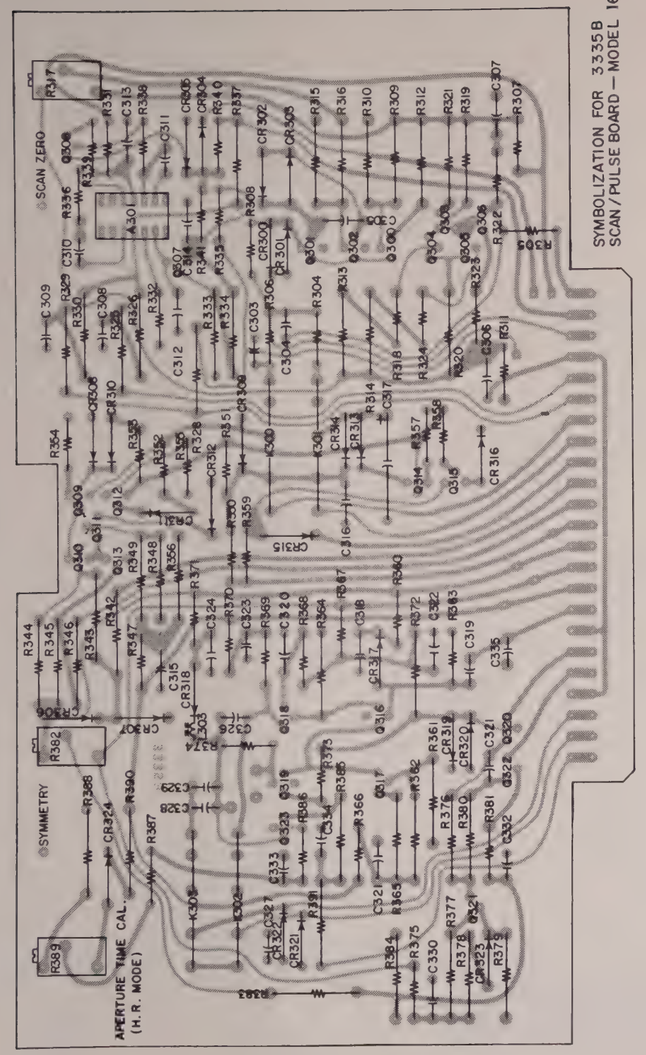
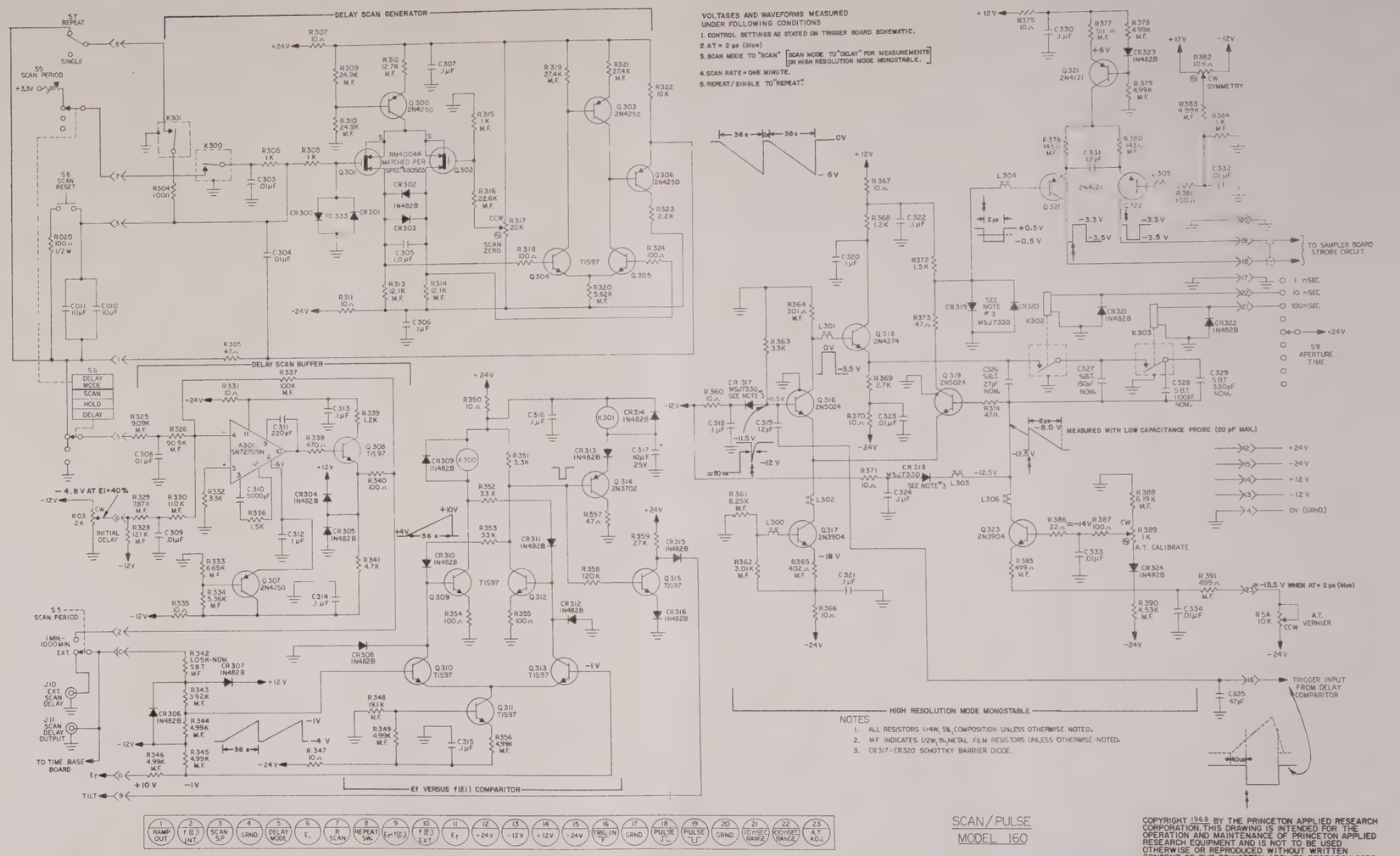
3330 D SD G

SYMBOLIZATION FOR 3335B
SCAN / PULSE BOARD — MODEL 160





VOLTAGES AND WAVEFORMS MEASURED UNDER FOLLOWING CONDITIONS

1. CONTROL SETTINGS AS STATED ON TRIGGER BOARD SCHEMATIC.
2. A.T. = 2 μs (blue)
3. SCAN MODE TO "SCAN" [SCAN MODE TO "DELAY" FOR MEASUREMENTS ON HIGH RESOLUTION MODE MONOSTABLE.]
4. SCAN RATE = ONE MINUTE.
5. REPEAT / SINGLE TO "REPEAT."

NOTES

1. ALL RESISTORS 1/4W, 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. M.F. INDICATES 1/2W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. CR317-CR320 SCHOTTKY BARRIER DIODE.

SCAN / PULSE
MODEL 160

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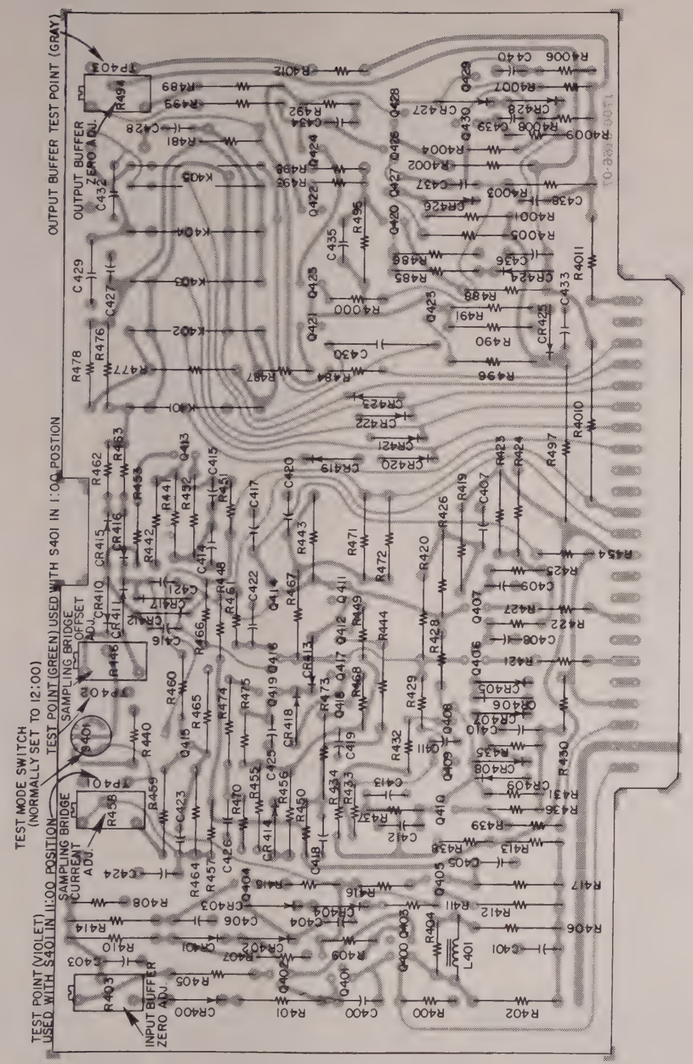
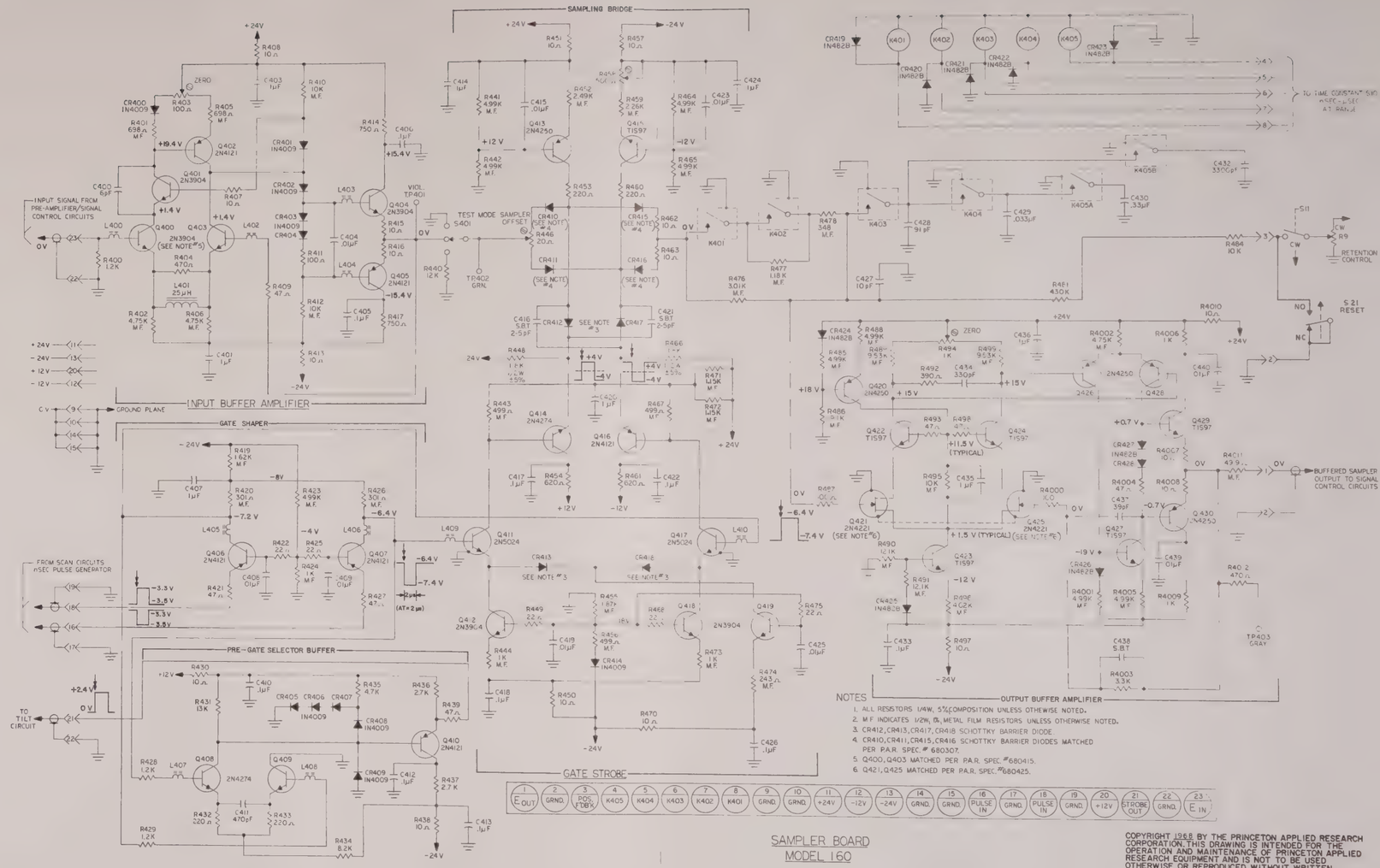
SYMBOLIZATION FOR 3426
SAMPLER BOARD — MODEL 160


OUTPUT BUFFER TEST POINT (GRAY)
OUTPUT BUFFER ZERO ADJ.
TEST MODE SWITCH (NORMALLY SET TO 12:00)
TEST POINT (GREEN) USED WITH S401 IN 11:00 POSITION
SAMPLING BRIDGE OFFSET ADJ.
SAMPLING BRIDGE CURRENT ADJ.
TEST POINT (VIOLET) USED WITH S401 IN 11:00 POSITION
INPUT BUFFER ZERO ADJ.



SAMPLER BOARD
MODEL 160

NOTES

1. ALL RESISTORS 1/4W, 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. M.F. INDICATES 1/2W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. CR412, CR413, CR417, CR418 SCHOTTKY BARRIER DIODE
4. CR410, CR411, CR415, CR416 SCHOTTKY BARRIER DIODES MATCHED PER P.A.R. SPEC. # 680307.
5. Q400, Q403 MATCHED PER P.A.R. SPEC. #680415.
6. Q421, Q425 MATCHED PER P.A.R. SPEC. #680425.

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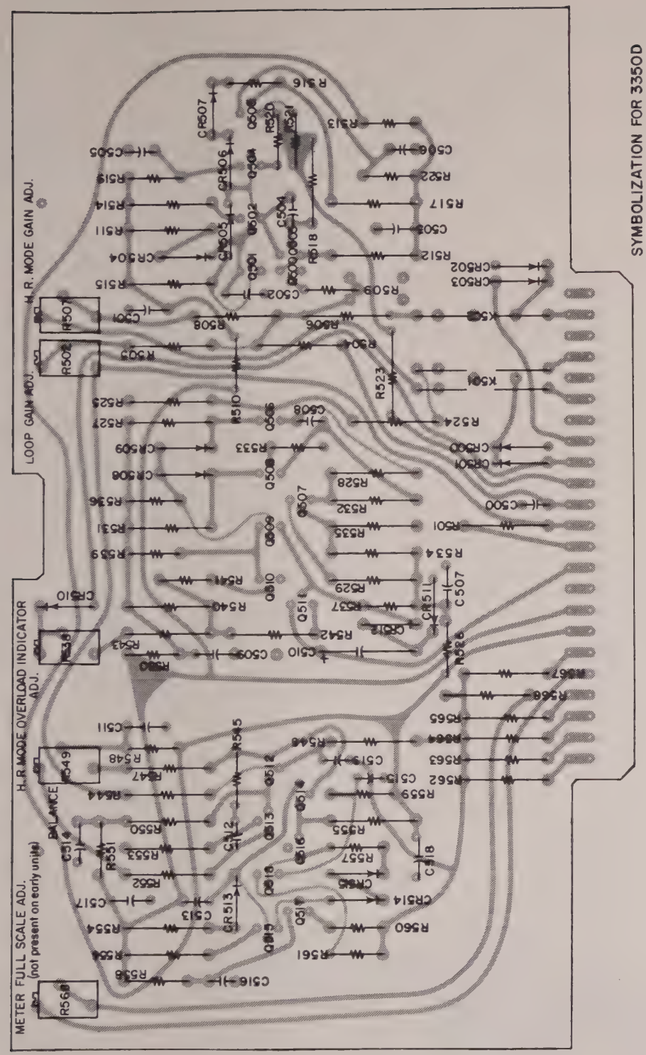
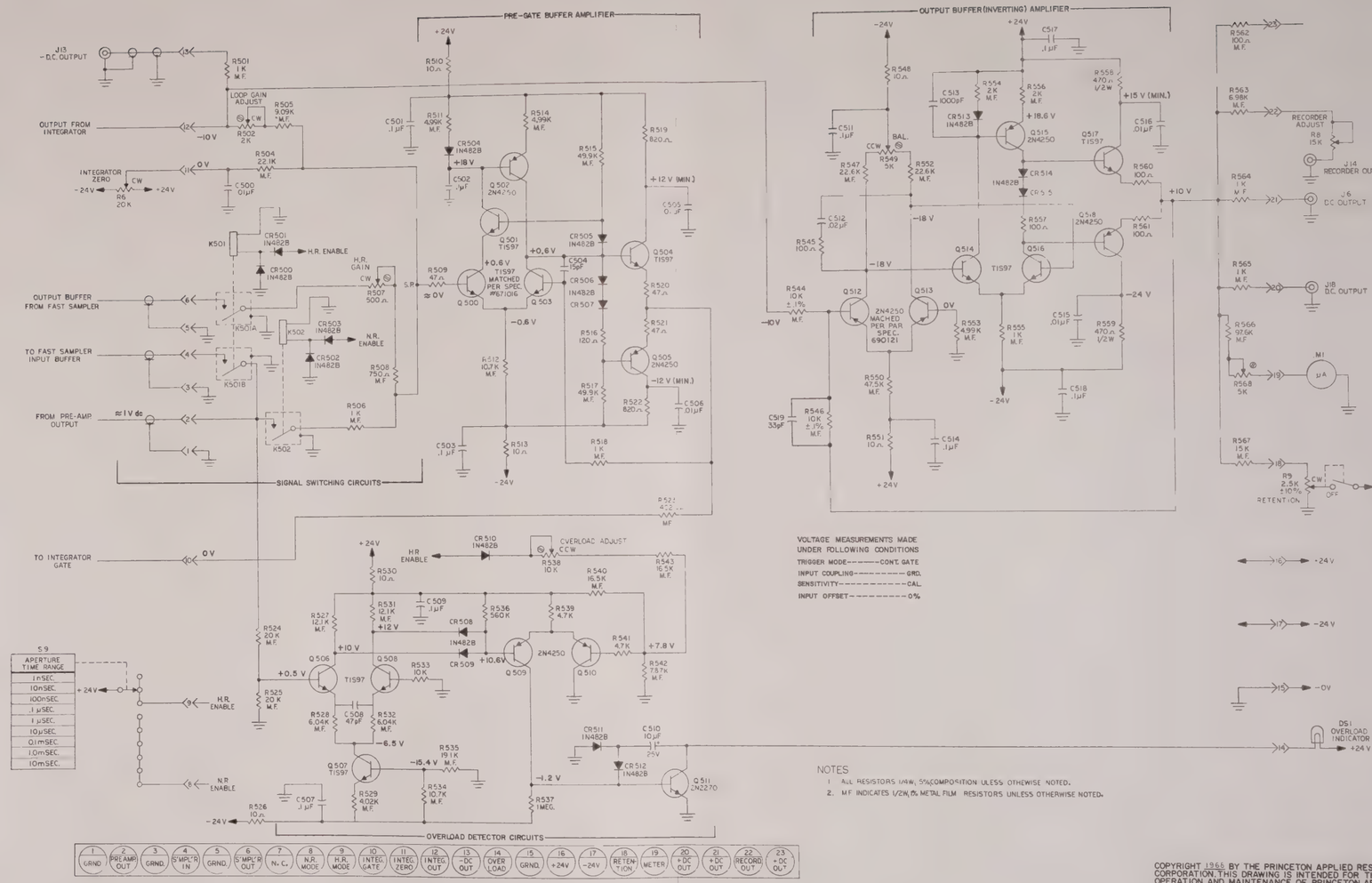
SYMBOLIZATION FOR 3350D
SIGNAL CONTROL BOARD—MODEL 160





SIGNAL CONTROL
MODEL 160

NOTES
1. ALL RESISTORS 1/4W, 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. M.F. INDICATES 1/2W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.

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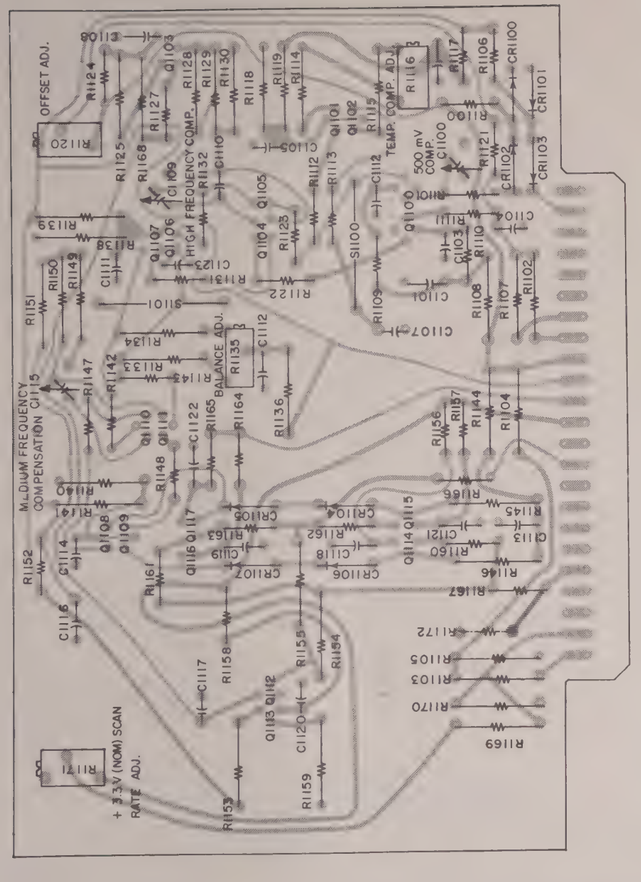
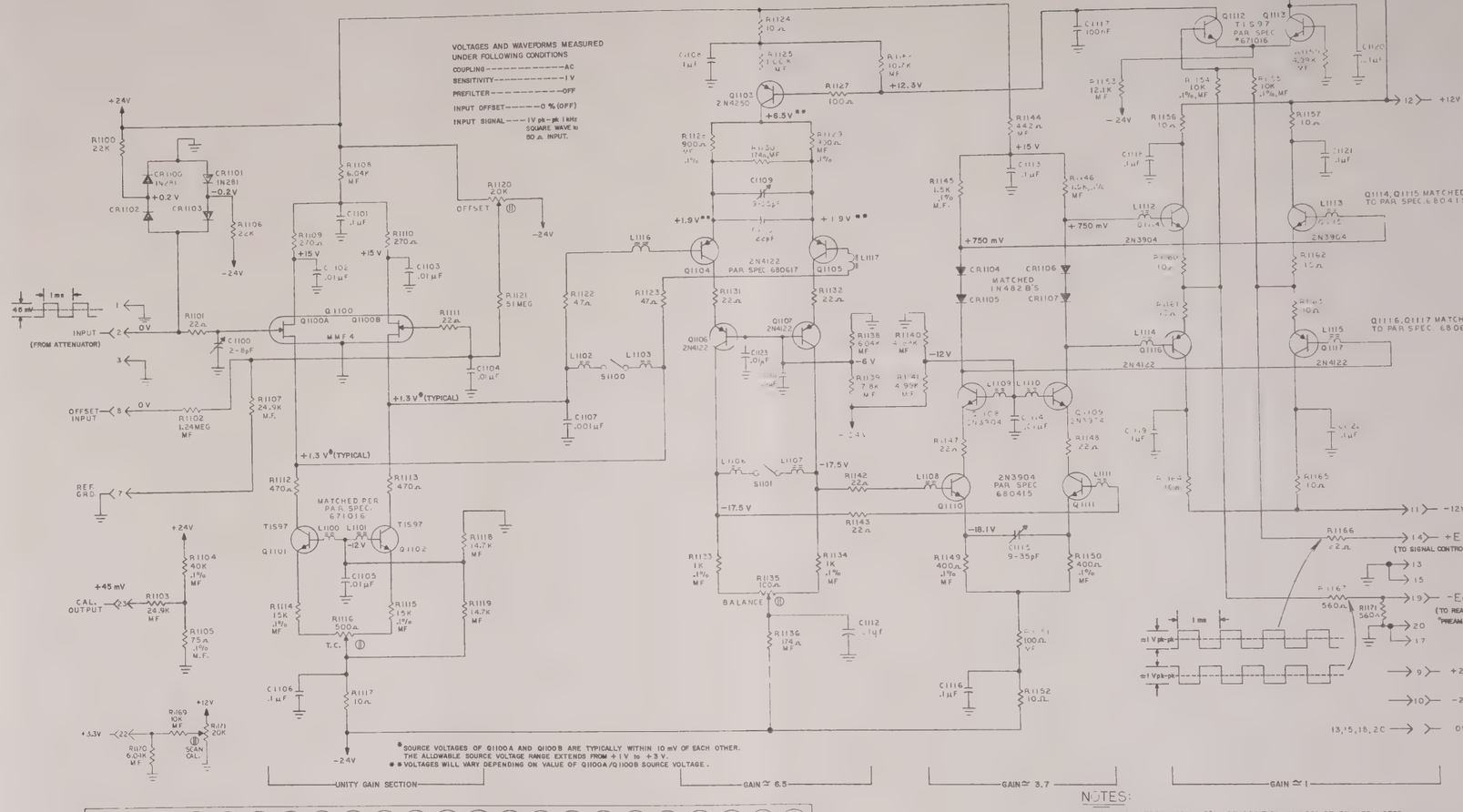


SYMBOLIZATION FOR 3524 B
PREAMPLIFIER BOARD — MODEL 160


VOLTAGES AND WAVEFORMS MEASURED UNDER FOLLOWING CONDITIONS
COUPLING ---------- AC
SENSITIVITY ---------- 1 V
PREFILTER ---------- OFF
INPUT OFFSET ------ 0 % (OFF)
INPUT SIGNAL --- 1V pk-pk 1 kHz SQUARE WAVE to 50 Ω INPUT.
*SOURCE VOLTAGES OF Q1100A AND Q1100B ARE TYPICALLY WITHIN 10 mV OF EACH OTHER. THE ALLOWABLE SOURCE VOLTAGE RANGE EXTENDS FROM +1 V to +3 V.
**VOLTAGES WILL VARY DEPENDING ON VALUE OF Q1100A/Q1100B SOURCE VOLTAGE.
UNITY GAIN SECTION
GAIN ≃ 6.5
GAIN ≃ 3.7
GAIN ≃ 1
+12V
-12V
+E OUT
(TO SIGNAL CONTROL BOARD)
-E OUT
(TO REAR PANEL "PREAMP" OUTPUT)
+24V
-24V
0V

PREAMPLIFIER
MODEL-160

NOTES:
1. ALL RESISTORS 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. "MF" INDICATES 1/2W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. CR1104 & CR1105, CR1106 & CR1107 MATCHED WITHIN 10mV AT 10mA
4. CR1102, CR1103 SCHOTTKY BARRIER DIODES.

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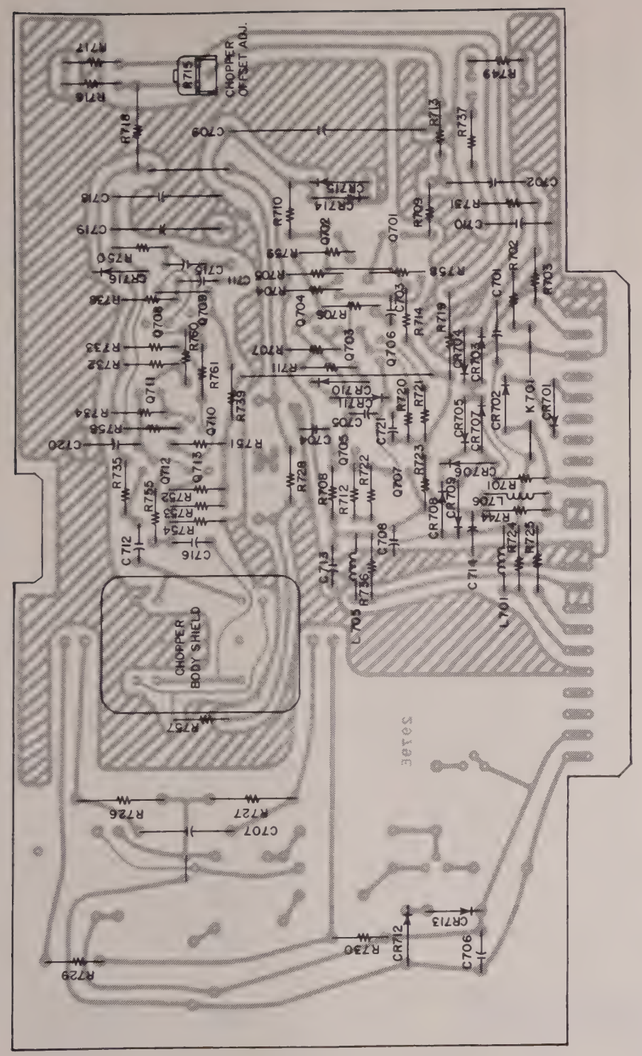
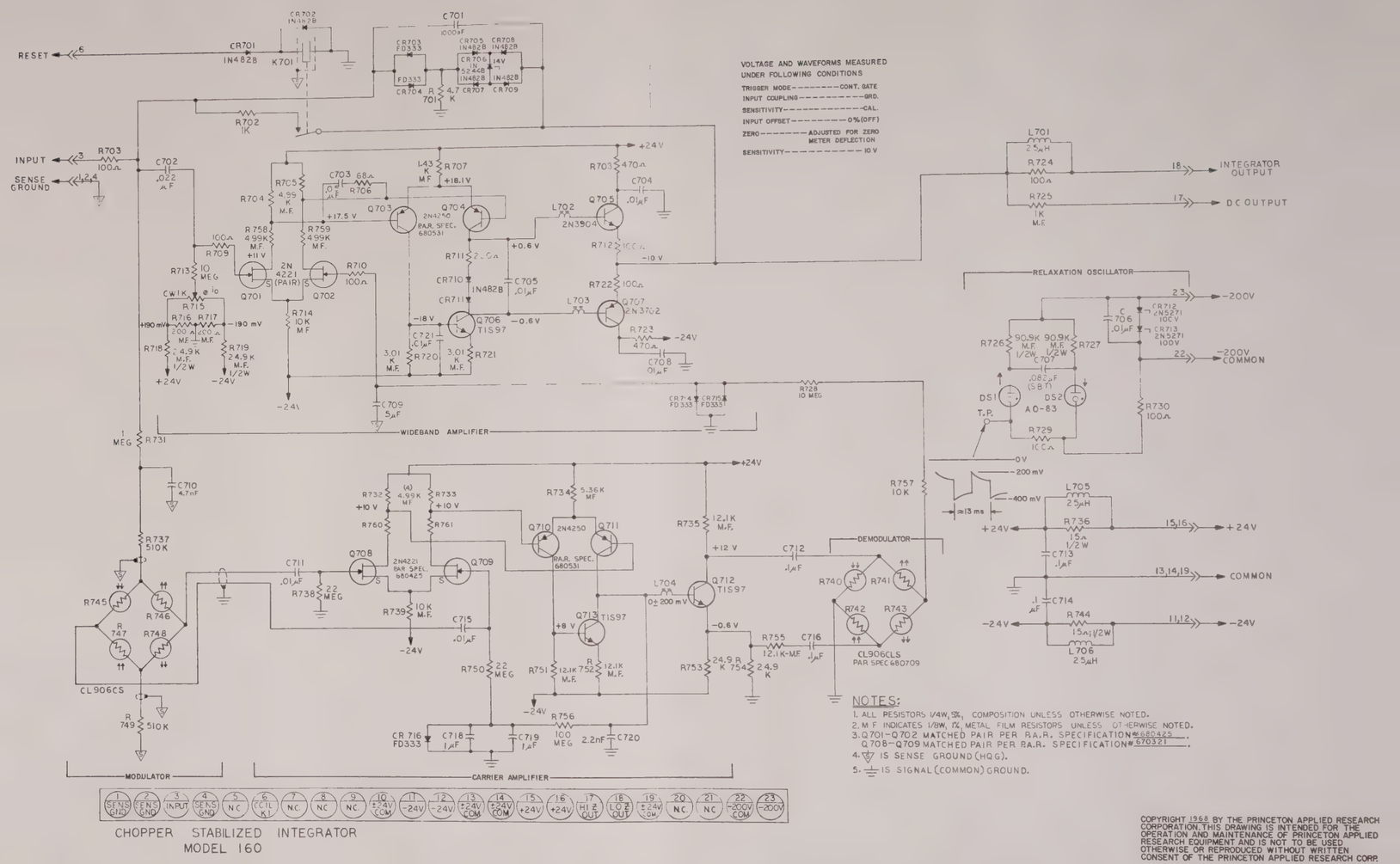


SYMBOLIZATION FOR 2979E
CHOPPER STABILIZED AMPLIFIER BOARD
MODEL 160



VOLTAGE AND WAVEFORMS MEASURED UNDER FOLLOWING CONDITIONS

TRIGGER MODE ---------- CONT. GATE
INPUT COUPLING ---------- GRD.
SENSITIVITY ---------- CAL.
INPUT OFFSET ---------- 0% (OFF)
ZERO ---------- ADJUSTED FOR ZERO METER DEFLECTION
SENSITIVITY ---------- 10 V

NOTES:

1. ALL RESISTORS 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. M F INDICATES 1/8W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. Q701-Q702 MATCHED PAIR PER P.A.R. SPECIFICATION #680423.
   Q708-Q709 MATCHED PAIR PER P.A.R. SPECIFICATION #.670321.
4. ▽ IS SENSE GROUND (HQG).
5. ⏚ IS SIGNAL (COMMON) GROUND.

CHOPPER STABILIZED INTEGRATOR
MODEL 160

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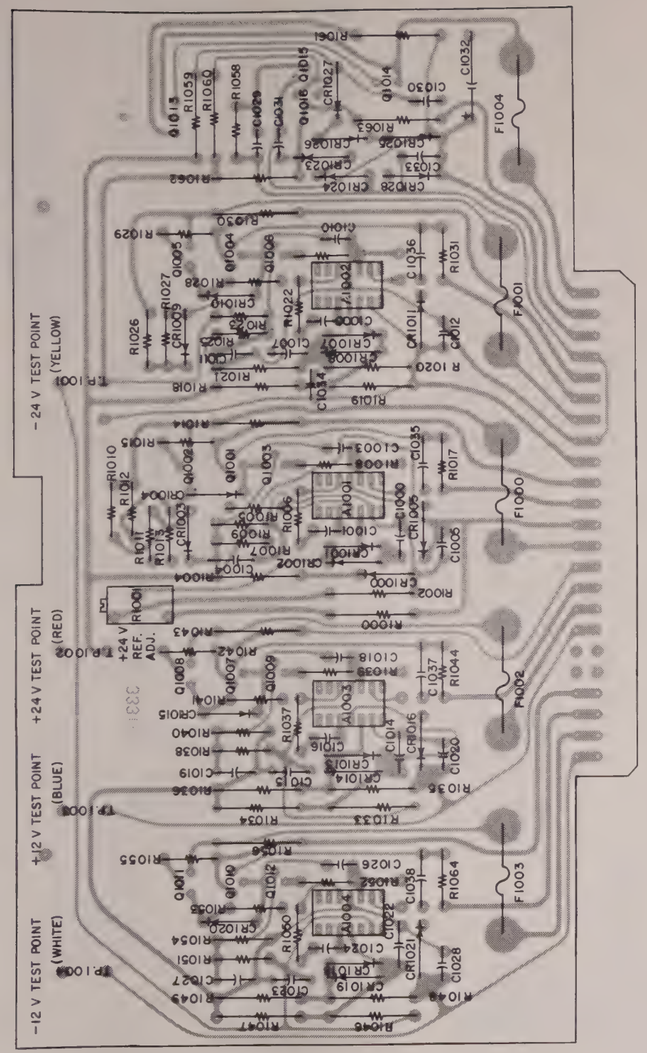
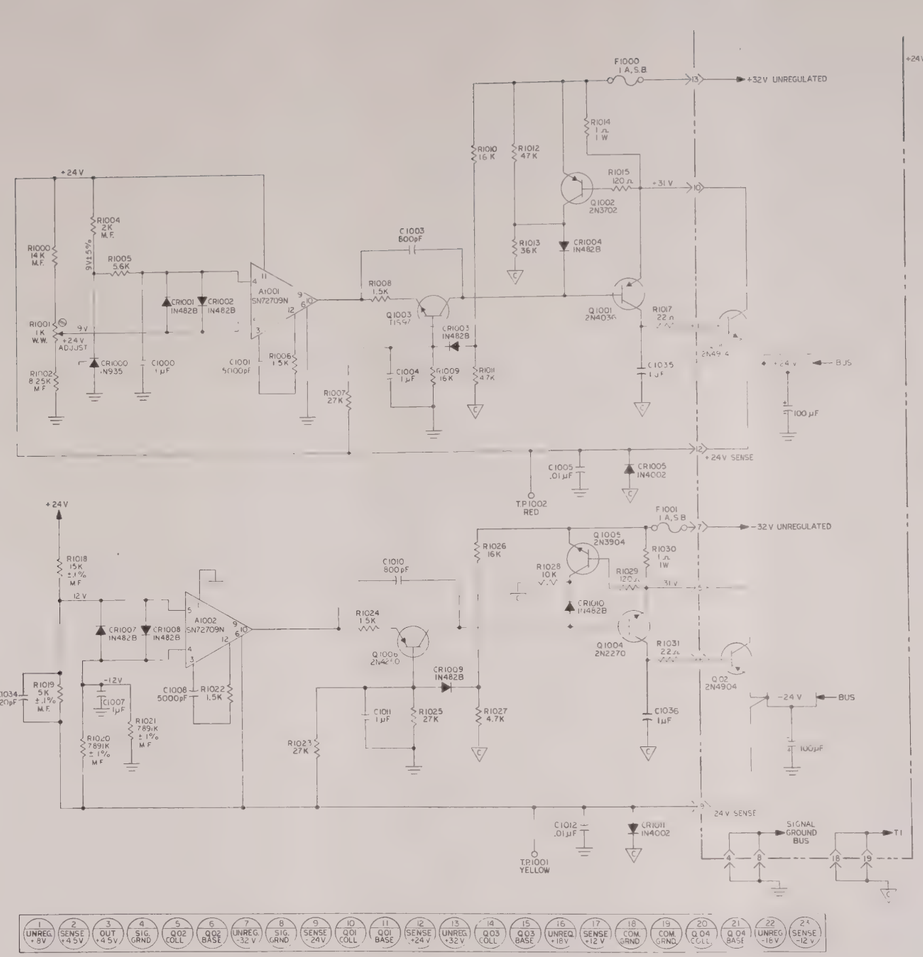
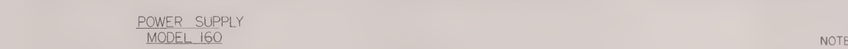
3264 D SDF

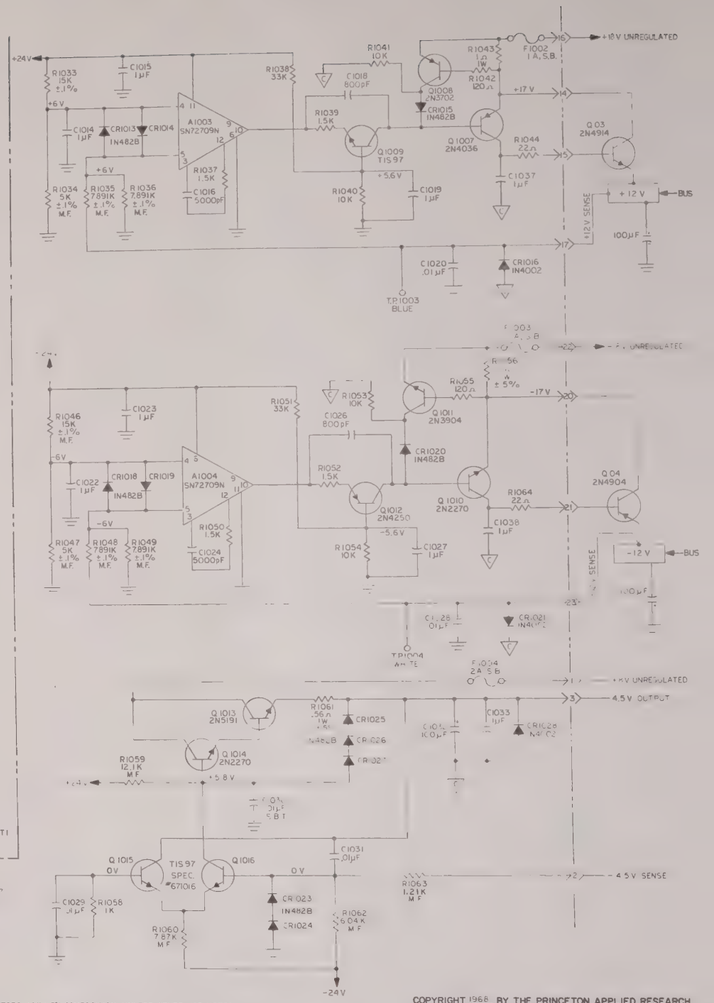
SYMBOLIZATION FOR 3331 B
POWER SUPPLY BOARD — MODEL 160







POWER SUPPLY
MODEL 160



NOTES
1. ALL RESISTORS 1/4W, 5% COMPOSITION UNLESS OTHERWISE NOTED.
2. M.F. INDICATES 1/2W, 1% METAL FILM RESISTORS UNLESS OTHERWISE NOTED.
3. ⏚ IS COMMON GROUND
4. ⏚ IS GROUND PLANE

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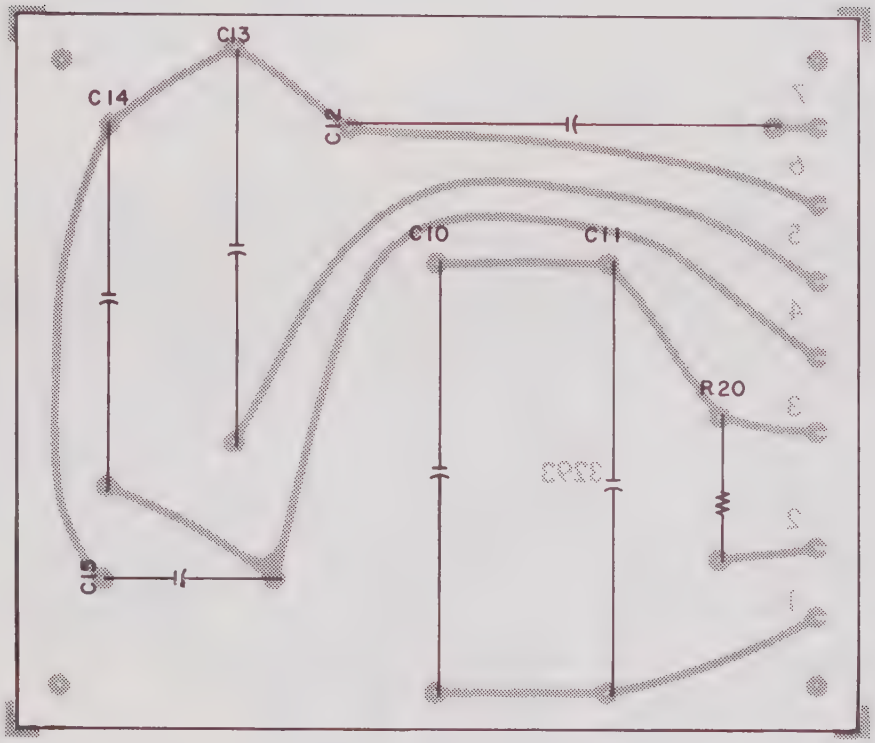
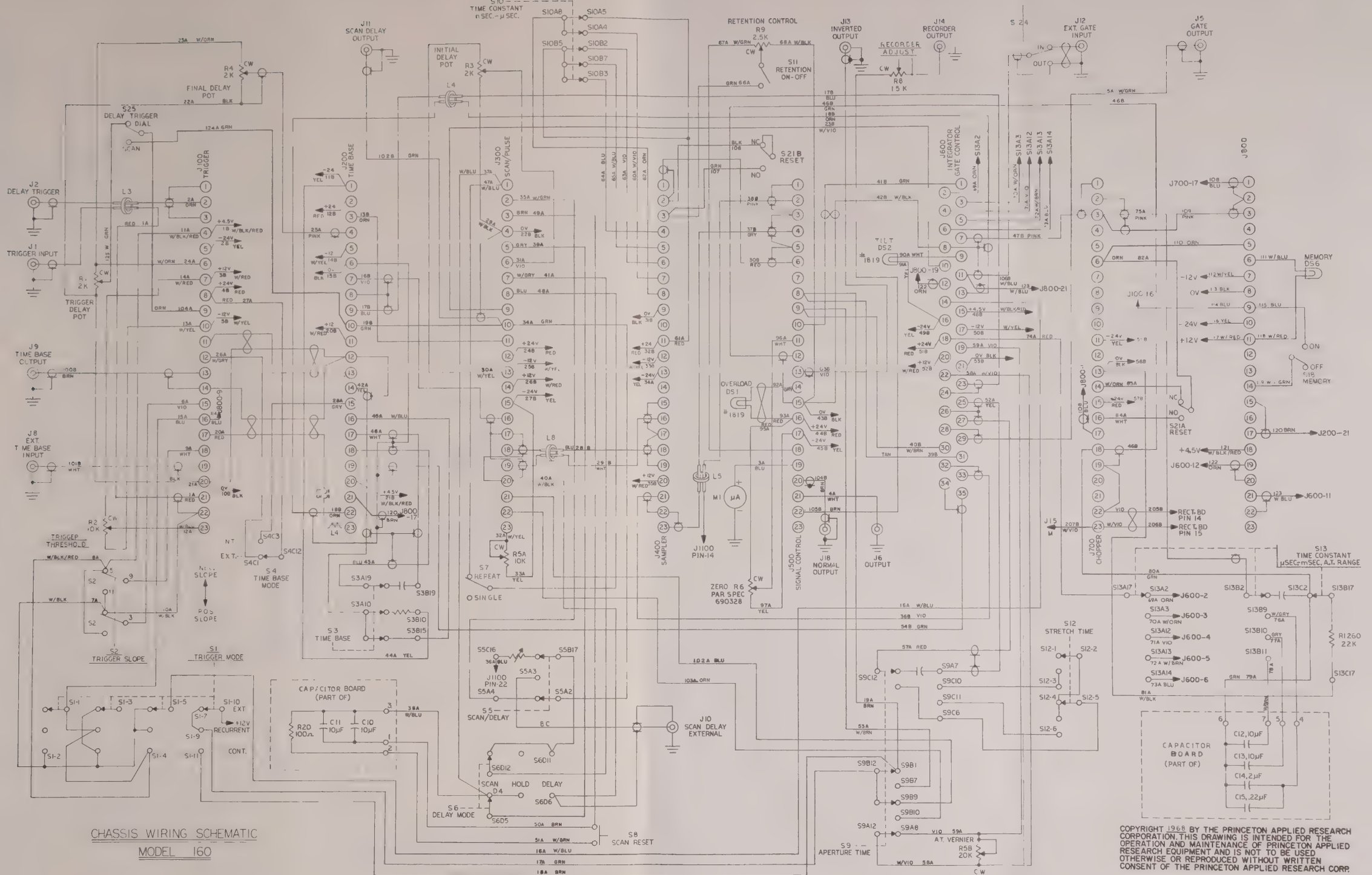


SYMBOLIZATION FOR 3291
CAPACITOR BOARD —— MODEL 160



CHASSIS WIRING SCHEMATIC

MODEL 160

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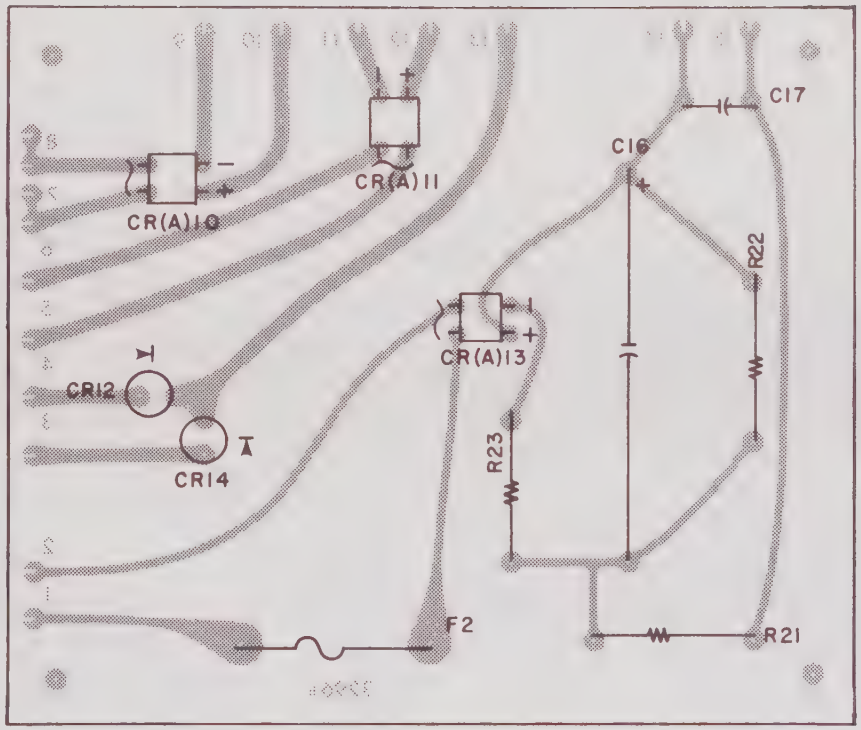
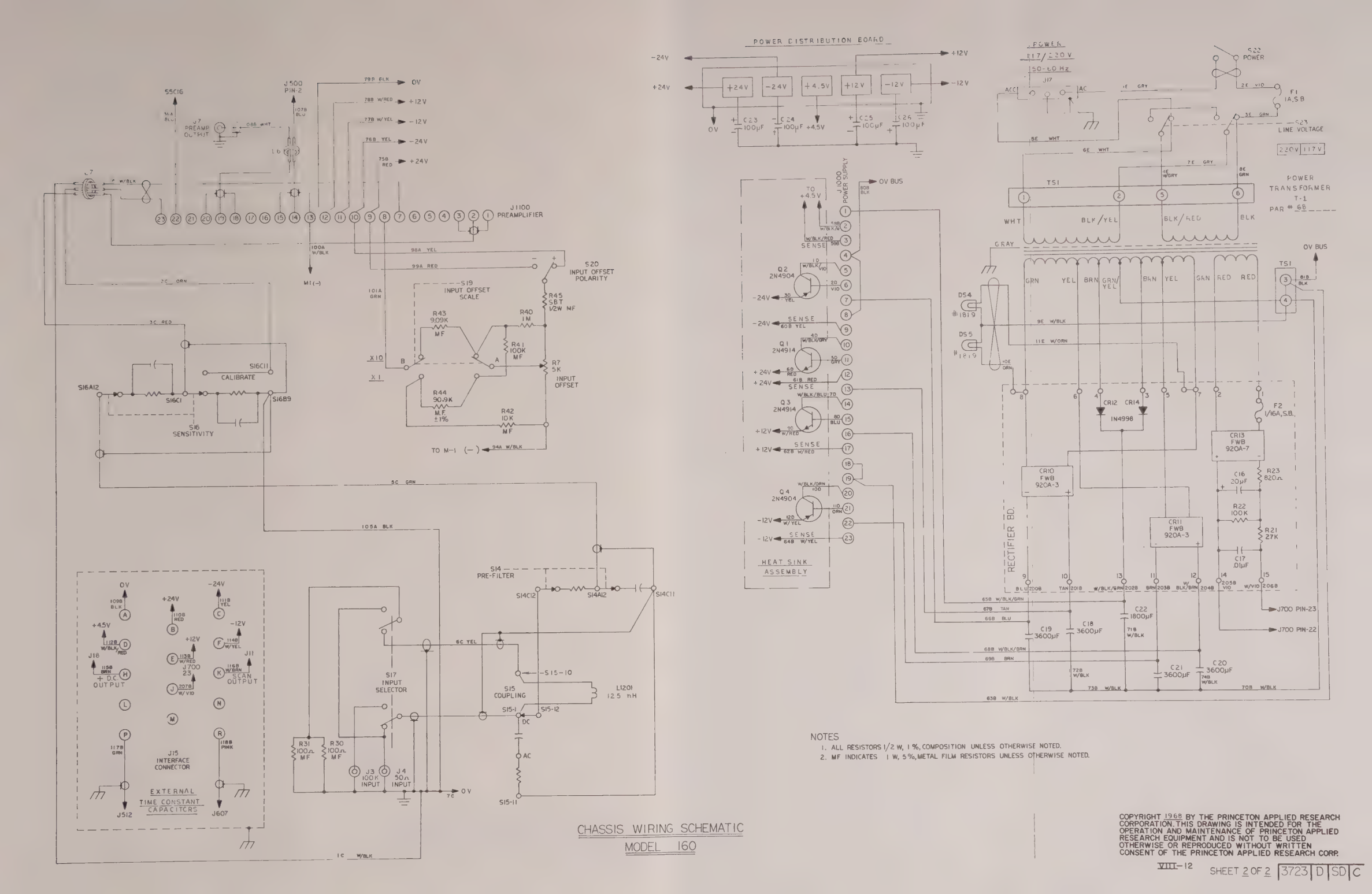


SYMBOLIZATION FOR 3294B
RECTIFIER BOARD —— MODEL 160



NOTES

1. ALL RESISTORS 1/2 W, 1 %, COMPOSITION UNLESS OTHERWISE NOTED.
2. MF INDICATES 1 W, 5 %, METAL FILM RESISTORS UNLESS OTHERWISE NOTED.

CHASSIS WIRING SCHEMATIC

MODEL 160

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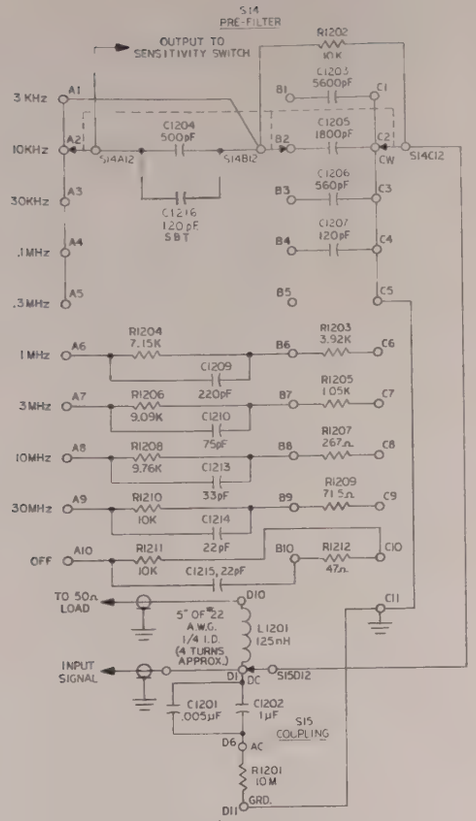
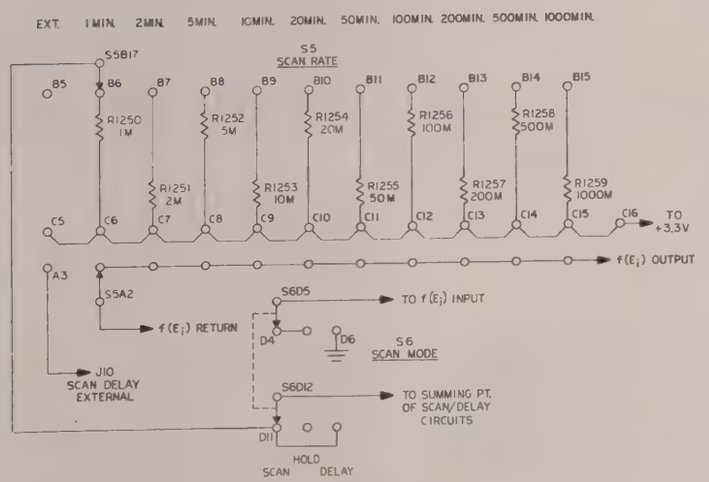
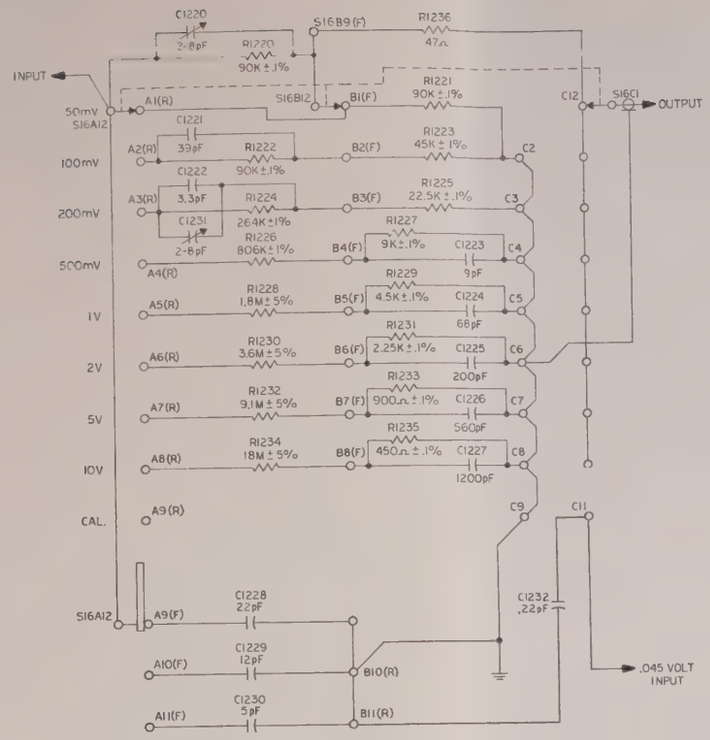


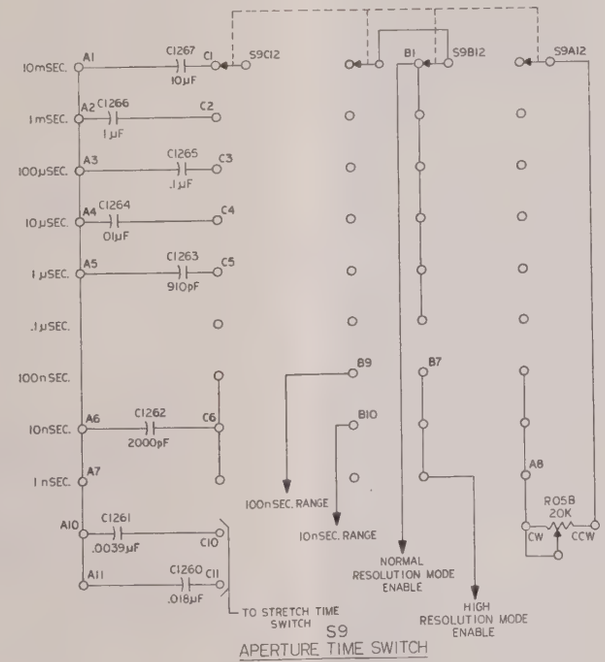
PRE-FILTER/COUPLING SWITCH
S14 & S15



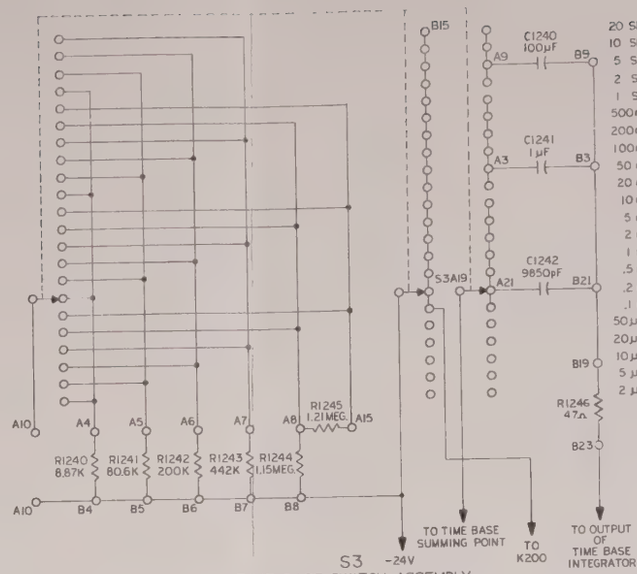
SCAN/DELAY SWITCH
S5 & S6



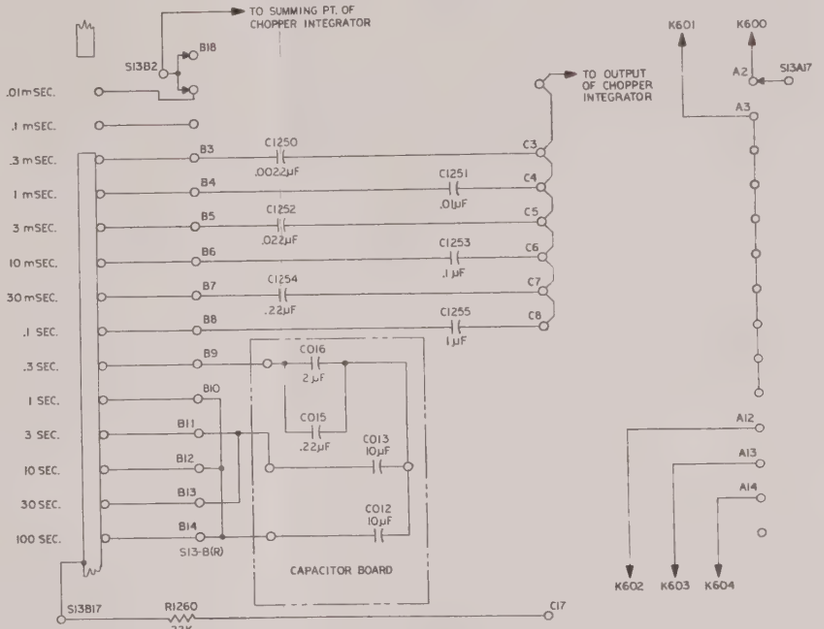
SENSITIVITY SWITCH
S16



S9
APERTURE TIME SWITCH



S3
TIME BASE SWITCH ASSEMBLY



TIME CONSTANT
μSEC.- mSEC. AT RANGE
S13

SWITCH SCHEMATIC
MODEL 160

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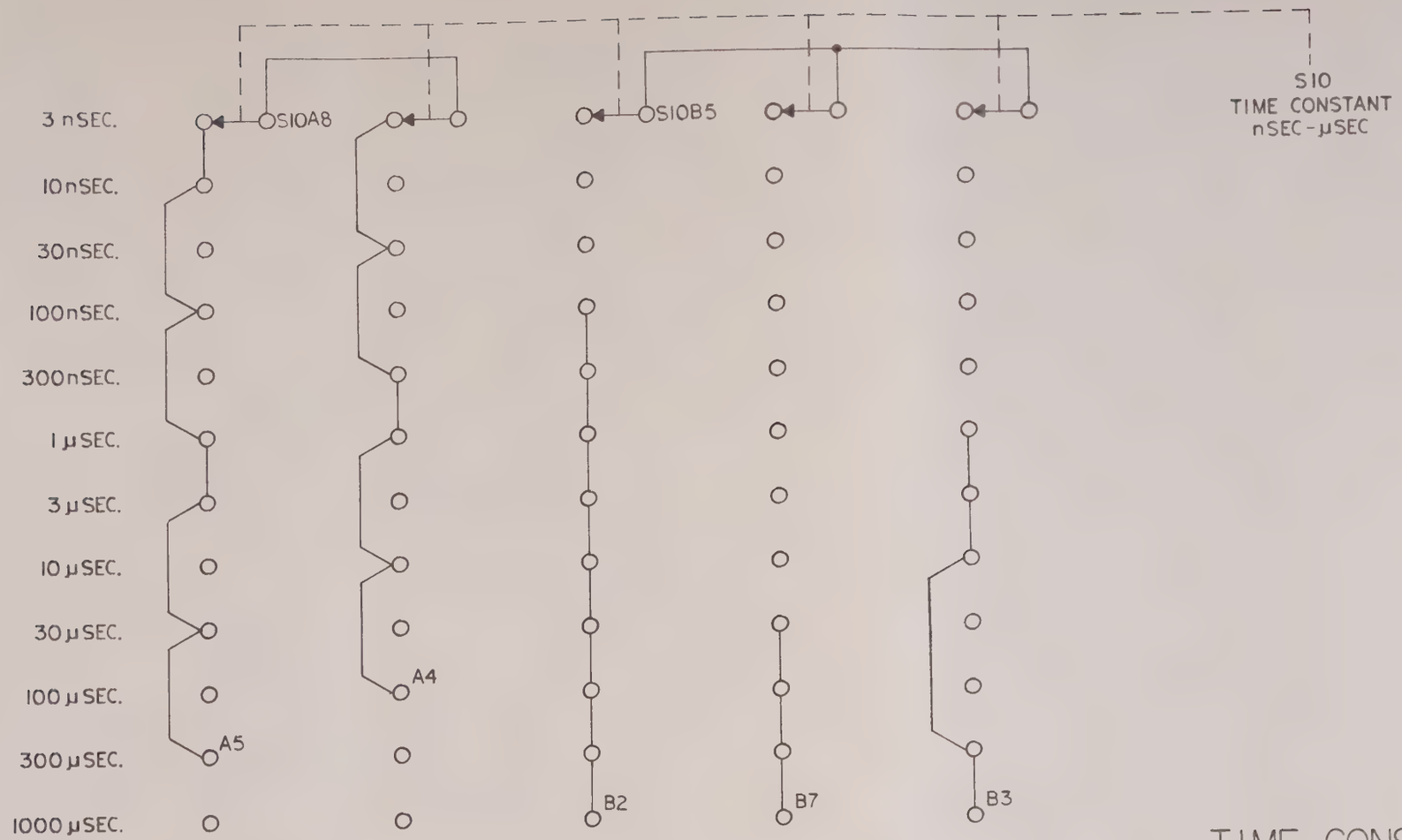

TIME CONSTANT SW. SCHEMATIC

MODEL 160

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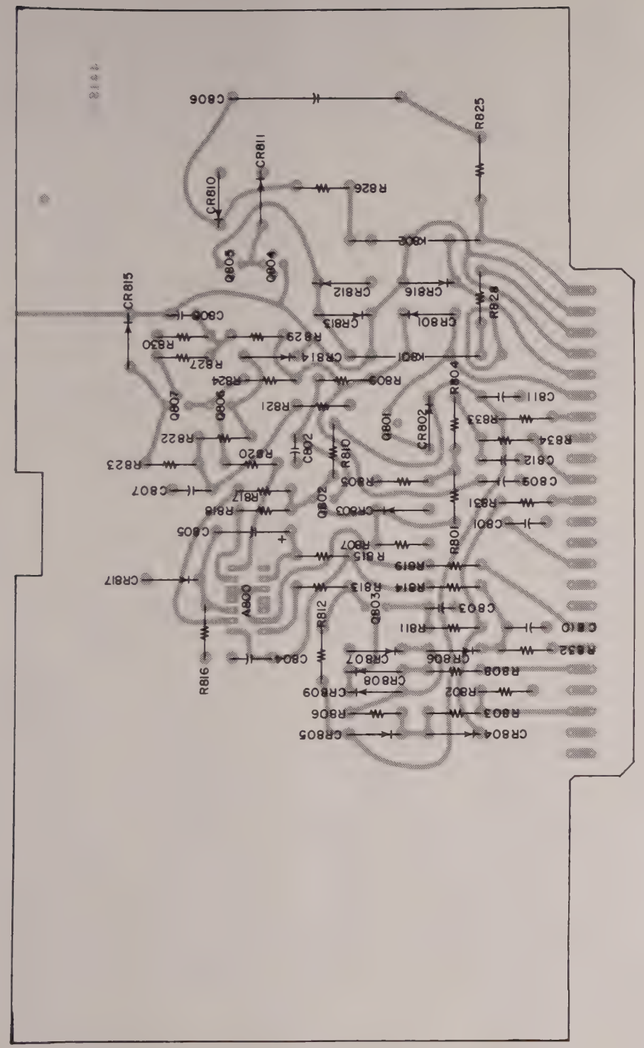
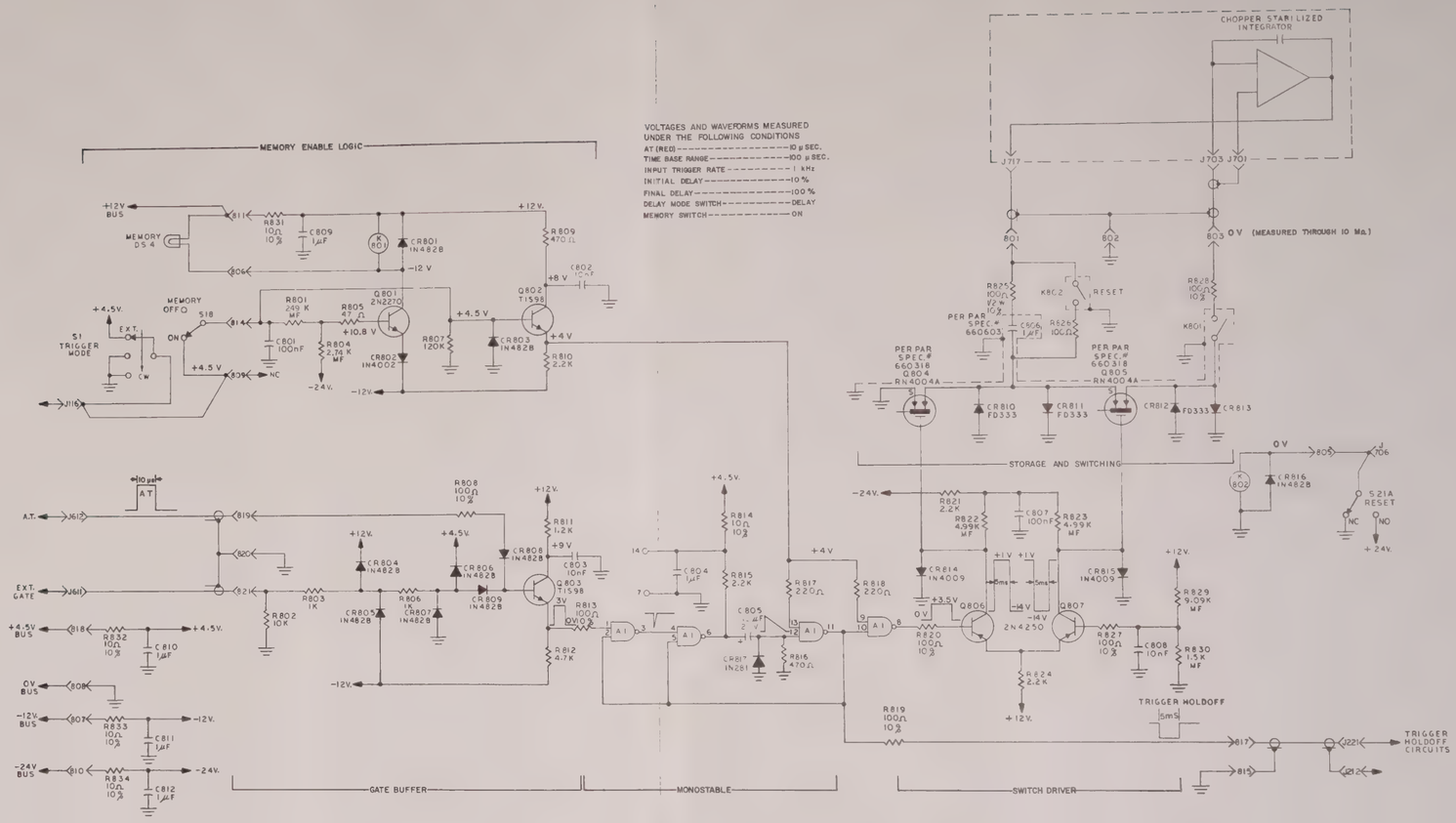


SYMBOLIZATION FOR 4418 A
ANALOG STORAGE ACCESSORY BOARD
MODEL 161



ANALOG STORAGE ACCESSORY BOARD

MODEL 161

NOTES:

1. ALL RESISTORS 1/4W, 5%, COMPOSITION UNLESS OTHERWISE NOTED.
2. MF INDICATES 1/8W, 1%, METAL FILM RESISTOR UNLESS OTHERWISE NOTED.
3. A1 IS A SN7400N.
4. Q804 & Q805 ARE SOCKET MOUNTED.

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TWX: 910-760-1708

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